Bidirectional Three Phase Power Converter

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Abstract— **This research aimed to design a three-phase ac-dc buck converter to achieve low-THD unity-power-factor sinusoidal input current and regulated dc voltage via modified pulse-width-modulation (PWM) technique. A 6-switch topology with bidirectional power flow capability is presented. The modified PWM switching strategy is discussed and verified via Matlab-Simulink and implemented in Digital Signal Processor (DSP) TMS320F28335. The topology and the switching technique performed well for sinusoidal input current, power factor, harmonic distortion level of the ac input currents, and regulated dc voltage, and enabled return of power flow from the dc side back to the ac. Simulation using Matlab-Simulink is presented to verify the effectiveness of the circuit configuration.**

Keywords- bidirectional; three-phase power converter; modified PWM; DSP

I. INTRODUCTION

A comprehensive review on three phase ac-dc converters has been done on the configuration using IGBTs as a replacement of the conventional diodes rectifiers. These converters have been extensively developed to improve power quality. The main feature of the improved power quality are described as nearly sinusoidal input current, regulation of input power factor to unity, low harmonic distortion of line current (based on standards such as IEEE 519, IEC-1000 and IEC 61000-3-2 [1-2]), adjustment and stabilization of DC-link voltage (or current) and reduced capacitor (or inductor) size due to the continues current.

Rectifiers are nonlinear system, generating harmonic current into the ac line power. High harmonic content in line current causes low power factor in a load and problems such as voltage distortion and electromagnetic interference (EMI) in power distribution systems, affecting power-system users and increasing volt-ampere ratings of power-system equipment such as generators and transformers. The topologies can be divided into two main categories: unidirectional and bi-directional. Three phase ac-dc converter configurations for unidirectional that use various switching techniques for control of power has been proposed in [3]. The most widely used is pulse width modulation (PWM), which requires high switching frequency, for wide bandwidth and small inductor-current ripple. The bidirectional or regenerative rectifiers using PWM technique had been discussed in [4].

Some of the attractive features of buck rectifiers include the requirement for various controllable output dc voltage, inherent short-circuit, and easy in-rush current. One of the disadvatages of buck rectifier is that there is no path for reverse inductor current on the dc side, so modified PWM is required, for reverse-current flow path. The PWM switching scheme is discussed in [5-7] for PWM flyback converter (3-switch 12-diode rectifier) and implemented via FPGA. This paper focuses on three-phase PWM buck rectifier with bidirectional capability by improving the conventional six switches-six diodes buck rectifier topology. The bidirectional topology uses one carrier signal, instead of two carrier signal as discussed in [5, 6], to create the PWM gating signals for the switches. The modified PWM switching strategy is discussed and verified via Matlab-Simulink and implemented in DSP TMS320F28335.

The converter and the switching technique is designed to improve power quality, which is described as nearly sinusoidal input current, regulation of input power factor to unity, low harmonic distortion of line current (THD below 5%), and stabilization of DC-link voltage (or current).

II. CIRCUIT CONFIGURATION & PRINCIPLE OF OPERATION

A. *Circuit Configuration*

Two common topologies for three-phase buck rectifier using PWM to improve ac mains power quality and output dc bus [5-12] as shown in Fig.1. Topology 1 is conventional 6-switch 6-diode and Topology 2 is modified 3-switch 12-diode, which has less driver-devices and less complicated PWM switching pattern. These topologies are classified as unidirectional. The topologies with capability of bidirectional power flow have been studied in [12-13].

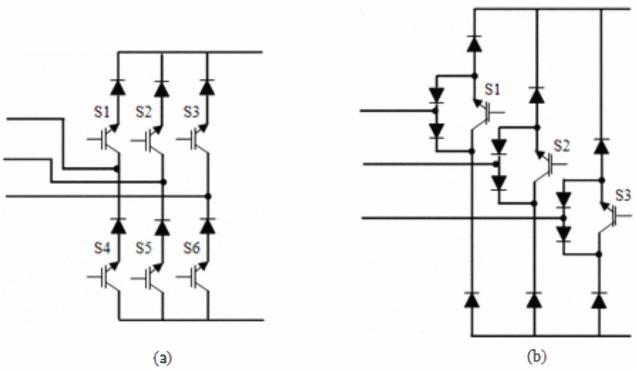

Figure 1. The topology's configuration (a) Topology 1 (b) Topology 2

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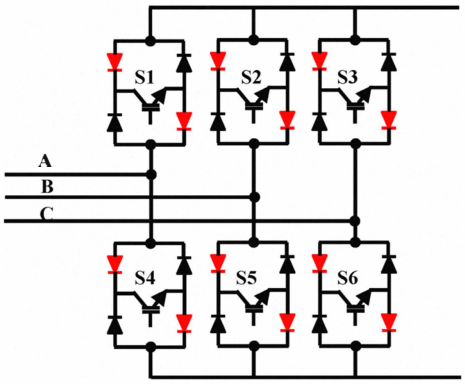

Figure 2. The topology's configuration

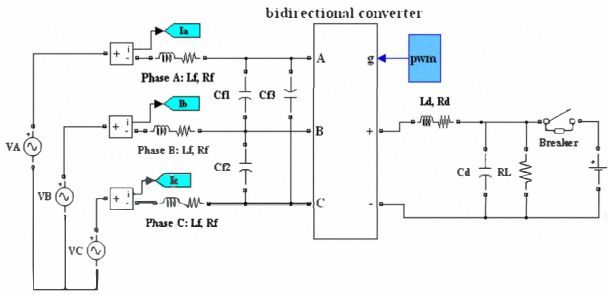

Figure 3. A rectifier's overall system drawn in Matlab-Simulink.

The circuit configuration in [13] is used in this paper (Fig. 2) with modification on switching technique to make it easier in constructing gating signals in DSP. Fig. 3 shows the three phase bidirectional system, drawn in Simulink-Matlab. There are two supply voltage, ac supply for rectifying mode and dc supply for inverting mode.

For the input filter, capacitor Cf is delta-connected, which, compared with star connection, gives good differential-mode performance and reduced resonant frequency. Parameters for the ac-side and dc-side filters are: (ac-side) Lf = 1 mH, Rf = 0.5 Ω, and Cf = 1 μF, and (dc-side) Ld = 2mH, Rd = 0.5 Ω, and Cd = 200 μF. Parameters for the snubber's (Rs-Cs circuit) IGBT and diode are Rs-Cs = 10 Ω -0.001μF.

The value of inductor, Ld for dc-side filter is obtained using equation:

$$Ld \geq (R_L(1-\frac{\sqrt{3}}{2}*M)*T_s) \div \frac{\Delta I_{L,ripple(\max)}}{I_L} \quad (1)$$

Where, R_L = 20 Ω (load resistance), M = 0.9 (modulation amplitude), T_s = $1/f_s$ = 1/19.8 kHz (sampling time), and $\frac{\Delta I_{L,ripple(\max)}}{I_L} \leq 15\%$. Using (1),

$$Ld \geq (20(1-\frac{\sqrt{3}}{2}*0.9)*1/19.8K) \div 0.15 \geq 1.5mH$$

Therefore, the chosen value for Ld is 2mH.

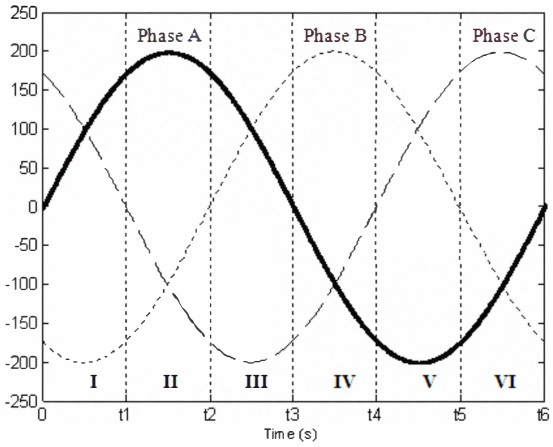

Figure 4. Three-phase supply-voltage waveforms (divided into six equal sections of the 360° mains cycle).

B. *Principle Of Operation*

Fig. 4 shows three-phase supply-voltage waveforms illustrating the rectifier/inverter principle of operation for PWM switching [6]. The IGBT switching is divided into six equal sections of the 360° mains cycle. Similar patterns repeat in each section, giving rise to the idea of designing only one PWM-pattern section. Positive cycle represents upper side of the switches (S1, S2, and S3) while the lower side switches (S3, S4, and S5) is represented by negative cycle. The technique reduces the number of power-device switching and reduces switching losses [14]. At any given time, only two converter legs are modulated independently, while another leg is in the 'on' state. Voltage and current waveforms can be expressed as follows:

$$Va = V_m \sin \omega t \quad (2)$$

$$Ia = I_m \sin(\omega t + \phi) \quad (3)$$

$$Vb = V_m \sin(\omega t - \frac{2\pi}{3}) \quad (4)$$

$$Ib = I_m \sin(\omega t - \frac{2\pi}{3} + \phi) \quad (5)$$

$$Vc = V_m \sin(\omega t + \frac{2\pi}{3}) \quad (6)$$

$$Ic = I_m \sin(\omega t + \frac{2\pi}{3} + \phi) \quad (7)$$

Where, V_m is peak voltage, I_m is peak current, and ϕ is the angle between phase voltage and current or displacement factor. Each section has three modes of circuit operation. Equations for current flow and bridge voltage (V_L) for the switch combinations in section 1are as follows:

Mode 1: $Ia = I_L*M*T_a$, $Ib = -Ia$, $Ic = 0$, $V_L = Vab$ (8)
Mode 2: $Ia = 0$, $Ib = -Ic$, $Ic = I_L*M*T_b$, $V_L = Vcb$ (9)
Mode 3: $Ia = 0$, $Ib = 0$, $Ic = 0$, $V_L = 0$ (10)

$$V_L = \frac{3}{2} * M * V_m * \cos(\phi) \quad (11)$$

Mode 3 allows freewheeling current to flow on the dc side. The freewheeling path is formed when the modulated switches are off. Therefore the switch on the same leg must be turn 'on' to create freewheeling path for inductor current at dc side as shown in Fig. 5. The dc voltage V_{dc} is less than the bridge voltage by the drop R_d across the resistor. The voltage dc output voltage V_{dc} can be obtained using (12).

$$V_{dc} = \frac{3}{2} * M * V_m * \cos\phi * \frac{R_L}{R_L + R_d} \quad (12)$$

where, R_d is the equivalent series resistor (ESR) of the R_d.

Table I shows the commutating process during each topology's switching period T. Theoretically the dc voltage can be controlled between 0 and 1.5 times of the phase voltage peak V_m (in ideal condition where ϕ equals zero or unity power factor) as stated in (12).

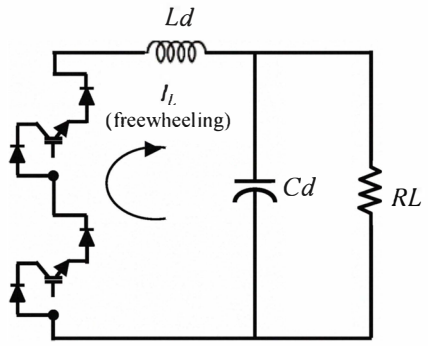

Figure 5. Freewheeling mode (Mode 3).

TABLE I. SWITCHING STATES OF SECTIONS I-VI

Section	Switches					
	S1	S2	S3	S4	S5	S6
I	T_a	T_f	T_b	T_{off}	T_{on}	T_{off}
II	T_{on}	T_{off}	T_{off}	T_f	T_b	T_a
III	T_b	T_a	T_f	T_{off}	T_{off}	T_{on}
IV	T_{off}	T_{on}	T_{off}	T_a	T_f	T_b
V	T_f	T_b	T_a	T_{on}	T_{off}	T_{off}
VI	T_{off}	T_{off}	T_{on}	T_b	T_a	T_f

III. PWM SWITCHING DESIGN

Five repeating similar patterns are generated for each switches, comprising modulated PWM (T_a and T_b), "on" state (T_{on}), "off" state (T_{off}) and "freewheeling" state (T_f) as shown in Table 1. Sixty-six samples of carrier signal of 19.8 kHz are generated in each section, resulted 396 samples of carrier signal to produce a 50Hz main frequency.

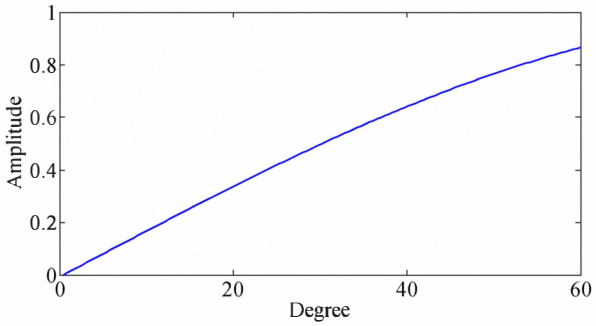

Figure 6. Reference signal consists of 132 data (for 60°).

A. *Generating the Look-up Table (reference signal)*

The 60° sinusoidal waveform (reference signal) look-up tables, as shown in Fig. 6, are used to generate modulated PWM T_a. Modulated PWM T_b is obtained by manipulating the look-up table of the reference signal. The PWM is based on asymmetrical switching technique, generating 132 data of reference signal stored in the look-up table. The modulation index can be controlled from 0 to 1 by multiplying the value with the reference's look-up table.

B. *Generating the Gating Signals*

The process of generating PWM for a 50Hz main frequency using asymmetrical switching technique is shown in Fig. 7. DATA is the reference look up table, i refers to the number of look up table's data, Zero and PRD occur when carrier's signal value is zero and maximum, respectively.

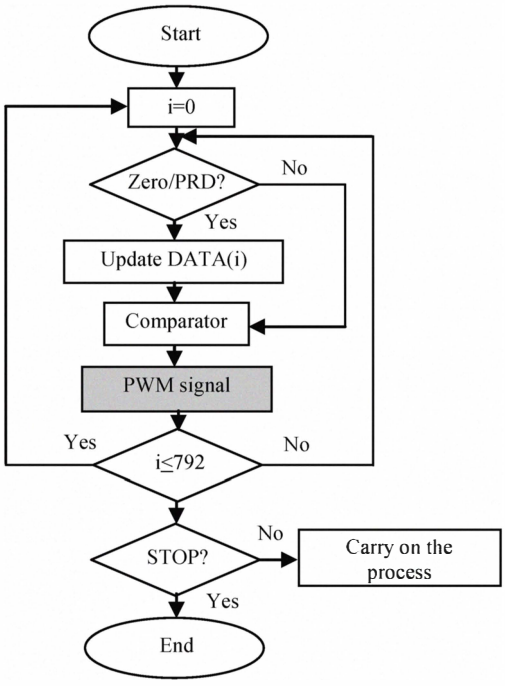

Figure 7. The process on generating PWM signals using assymmetrical switching technique.

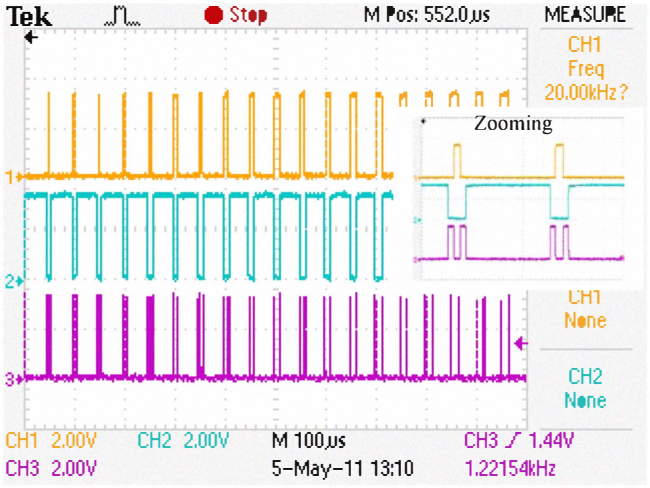

Figure 8. PWM signals generated via DSP.

The references signals are compared with carrier signals, respectively to generate PWM T_a, PWM T_b, and PWM T_f patterns. Fig. 8 shows the PWM signals generated via DSP. Zooming illustrate the PWM T_f (bottom) is "on" when both PWM T_a (upper) and T_b (middle) are "off".

Fig. 9(a) and (b) show the PWM pattern of 50Hz main frequency via DSP (captured by oscilloscope) for switches S1, S4, S2, S5, and simulation MATLAB for switches S1-S6.

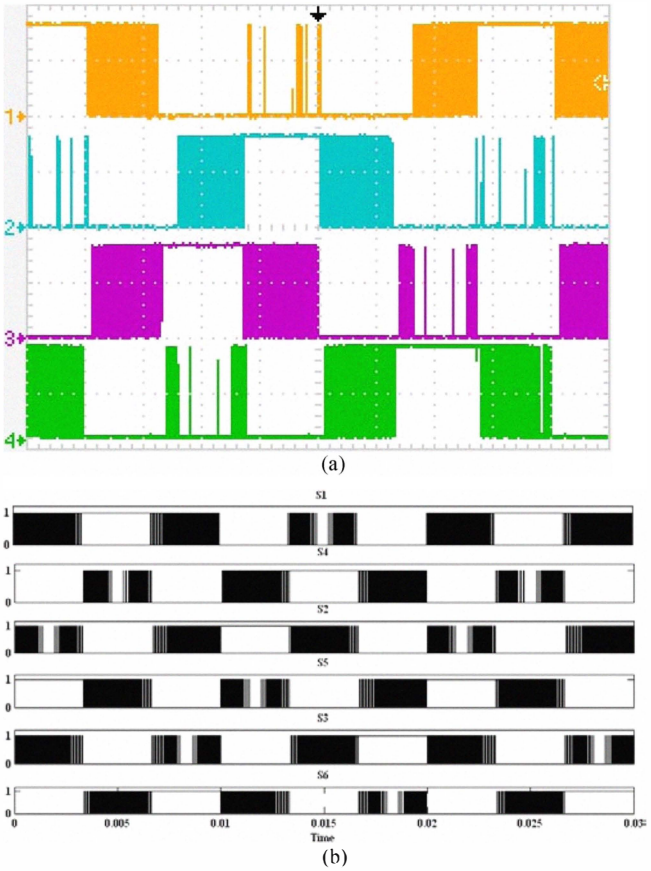

Figure 9. PWM pattern (modulation index=1.0) via (a) DSP (b) MATLAB

IV. Simulation Results

Specifications for the IGBTs and the diodes are:

IGBT: Ron = 0.001Ω, Lon = 0, forward voltage = 1V, current 10% fall time = 1µs, current tail time = 2µs
Diode: Ron = 0.001Ω, Lon = 0, forward voltage = 0.8V.

Part II describes the design of the input and the output filters. Figs. 10-13 show the input current in phases A, B, and C, the FFT analysis graph for input current (phase A), the dc voltage (V_{RL}) with output current I_L, the bridge voltage V_{bridge} of each topology and, with these specifications: input voltage V_{in} = 200V (Vpeak for Phases A, B, and C), modulation index M = 0.9, and load resistance R_L = 20Ω. These figures demonstrate the proposed topology obtained near-unity power factor (0.99) with a good THD value (less than 5%), regulated dc output voltage at steady-state (250V), and stable bridge voltage (dc voltage before filtering), when operated in rectifying mode. The efficiency of the system is calculated 89.3%.

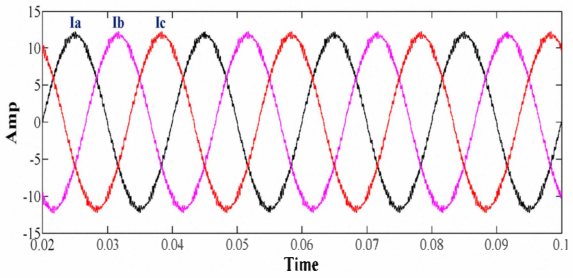

Figure 10. The input current of phases A, B, and C of each converter

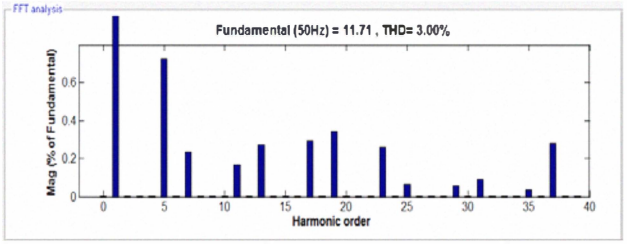

Figure 11. FFT analysis for input current (Phase A)

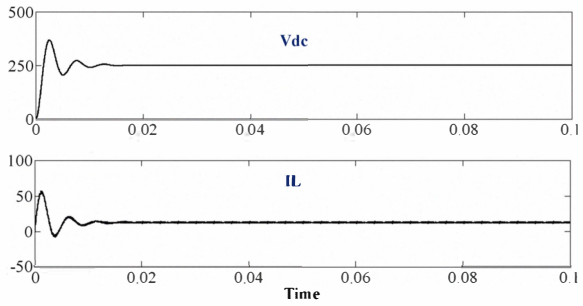

Figure 12. The dc voltage with output current I_L

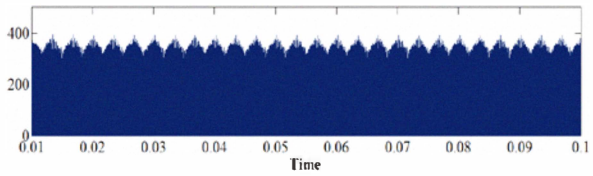

Figure 13. The bridge voltage V_L before filtering

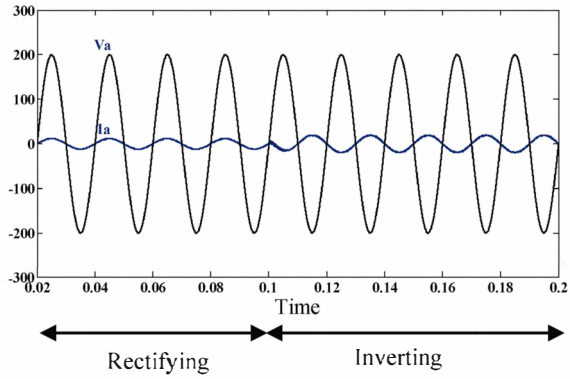

Figure 14. The input current and voltage for phase A for rectifying and inverting modes

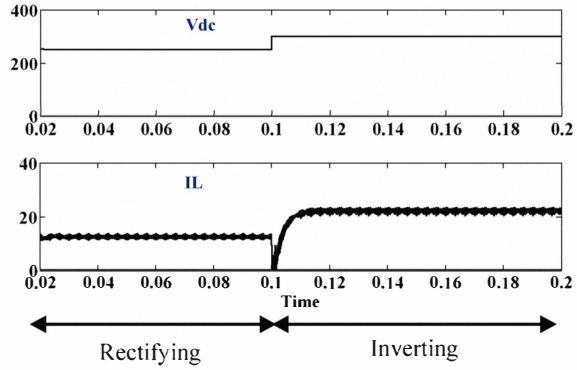

Figure 15. The dc voltage with output current I_L

Figs. 14-15 show simulation results of input current and voltage at ac side for phase A and the dc voltage across R_L with inductor current at dc side, for rectifying and inverting modes.

V. Discussion & Future Works

The three phase bidirectional circuit topology which uses six switches is presented (fewer switches than a conventional anti parallel converter). Modified PWM switching is shown to improve power quality of ac-dc buck rectifier. It provides a sinusoidal input current, near-unity power factor, low harmonic distortion, regulated dc voltage, and a good percentage in efficiency. The proposed bidirectional topology is verified to perform well as rectifier and inverter via simulation. Improvement in controller design is needed to improve the transient response of dc current (rectifying mode). The intelligent controller needs to be investigated to resolve the conversion between rectifying and inverting modes.

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