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A low-phase-noise 18-GHz-band frequency synthesizer with low frequency step size

B. Biglarbegian [1,2], F. Hodjat Kashani[2], H. Ameri[3]
[1] *Iran University of science and technology, 2 Ameri_Tech telecommunication research company*
3 IT&MMWAVES.SDN.BHD
bbiglar@gmail.com, kashani@iust.ac.ir, itmmwave@streamyx.com

Abstract

Due to development of both wireless communication users and communication line users, utilization of high-speed communications has become a vital essence. High speed digital microwave radios have a great contribution in wireless telecommunications. Having a different and high capacitance, these radios can transmit and receive data in point to point links in far distances up to 30 km. Considering the high rate of utilization such digital microwave radios have in lower bands, it is imperative to utilize such kind of radios in upper bands for accessing more channels.

One of the radios that plays a significant role in communications is digital microwave radio 18 GHz. Through using a proper modulation in this band, transmitting data with high rate is achievable. In this paper, frequency synthesizer of this radio has been analyzed, designed and implemented. By applying proper changes, this synthesizer can be used as a frequency sweeper either. In this project in order to have a stable local oscillator and a good phase noise of output signal, a phase locked DRO was designed and implemented. This stable signal will be mixed with an L-band synthesized signal and it will generate signal in the band 17.7 GHz ~19.7 GHz with step 0.25 MHz. The stable output signal of this synthesizer has a very good phase noise at 18 GHz. We have achieved to phase noise up to -88 dBc/Hz @10 kHz in 18 GHz which is a proper phase noise for using different modulations such as QPSK, 16QAM, 64QAM and ...

1. Introduction

Designing a low phase noise and stable with low step size frequency synthesizer is a vital essence in a microwave link in different bands. For achieving a good phase noise we need a reference crystal oscillator with a very low phase noise in order to achieve a low phase noise either in the microwave band. Using a crystal oscillator with a higher frequency with the same phase noise as a lower frequency crystal oscillator, will provide lower phase noise, however this phase noise reduction will affect the step size of the synthesizer. For having a synthesizer with above specifications we can use either a mixing method or a dual-loop method. In mixing method two different phase-lock loops one with a very good phase noise and other with a low step size will generate the original signal. In the dual loop utilizing a dual loop with two phase detectors will generate both the good phase noise and the low step size. In this paper by using the mixing method we have implemented an 18 GHz frequency synthesizer. A block diagram of this synthesizer is shown in Figure 1. Using a 100 MHz as signal reference in a Phase locked Dielectric Resonator Oscillator (PLDRO) and in the reference of digital L-band synthesizer will achieve both low step size and low phase noise.

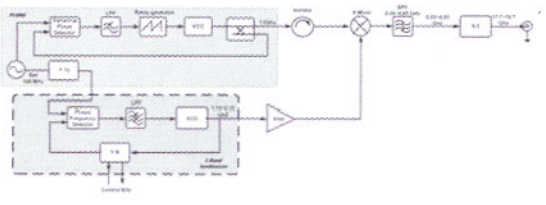

Figure 1: Block diagram of the Synthesizer

2. PLDRO

2.1. DRVCO

The most significant part of this oscillator is its VCO. Designing an X-band VCO with a DR as its resonator is a good choice because of its stability and its low voltage frequency gain [1,2]. A classical way to design a VCO is to use parallel half wave transmission lines, a DR between two lines, and an element which is

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capable of producing negative resistance attached to line number 2 as in Figure 2. [3-6]

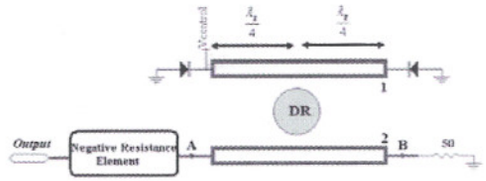

Figure 2: Schematic of DRVCO

In this implementation transmission line 1 is connected to two varactors. When a noise signal comes from Point A, it goes to point B through the 50 Ω resistance in the whole band except the resonance frequency of the dielectric resonator. In the resonance frequency of the DR, the signal coupled to the middle of the transmission line 1 where it encounters the open circuit condition, so the signal reflected completely and coupled to the transmission line 2 since the signal has a frequency just the same as the resonance frequency of the DR. There, in line No.2, the signal encounters a negative resistance of the transistor, so it will be reflected again with a gain more than one. This process continues till it results in oscillation.

The varactor diodes play an important role in this configuration, as the voltage changes the capacitance of the varactor diodes changes; the change in the capacitance of the diodes affects the electrical length of the transmission lines. In designing the DRVCO, We have modeled DR in HFSS as it shown in Figure 3.

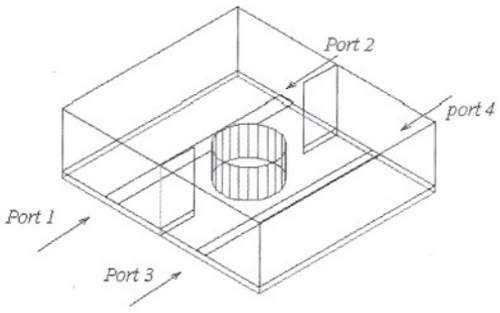

Figure 3: Modeling dielectric resonator in HFSS

As Figure 4 shows parameter S_{13} is the same as what we do expect—the signal can coupled just in the same frequency as the resonance frequency of the DR.

Now we can import the results of this configuration into the Microwave Office package. Port 2 is attached to a 50 Ω resistance, and ports No. 3 and 4 are attached to ground via a varactor which is modeled with a capacitor. Figure 5 shows a schematic view of this simulation in Microwave Office package.

In this stage we are seeking for parameter S_{11} and its changes. It can be seen that if the capacitance of the varactors varies between 1 pF and 5 pF, the oscillation frequency varies about 10 MHz around the center frequency 11 GHz.

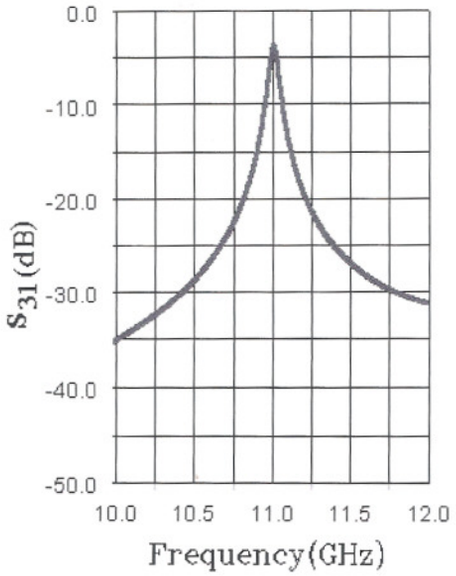

Figure 4: Coupling into port 3 from port 1 in resonance frequency of DR simulated in HFSS

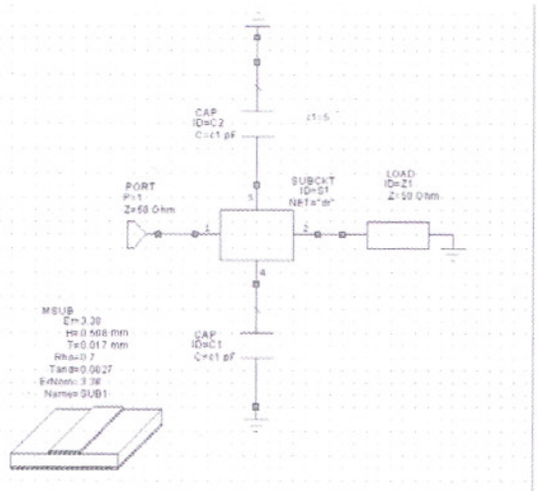

Figure 5: Schematic view of DRVCO simulated in Microwave Office package

To implement this configuration, a varactor whose capacitance varies between 1 pF and 5 pF is needed. We have used MA4STS560 from MA/COM company. The Transistor that is used as a negative resistance

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element must show negative resistance around 11 GHz. Figure 6 shows a view of the DRVCO on the test fixture.

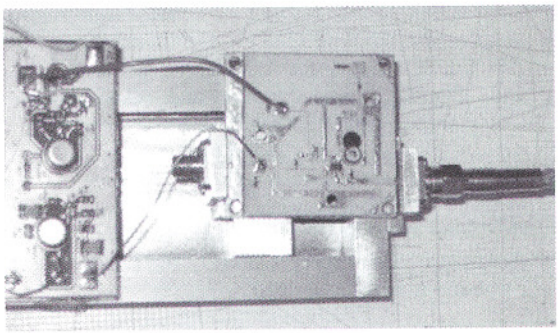

Figure 6: DRVCO on the fixture with bias circuit

2.2. SPD and loop design

Sampling Phase Detector(SPD) is a 5-port IC that consists of 2 schottky diodes, one SRD and 2 high frequency capacitors. The shottkies act as a mixer in phase comparing. The SRD acts as a frequency multiplier and capacitors will switch with the input signal from SRD. Figure 7 shows the SPD and the elements inside it [7].

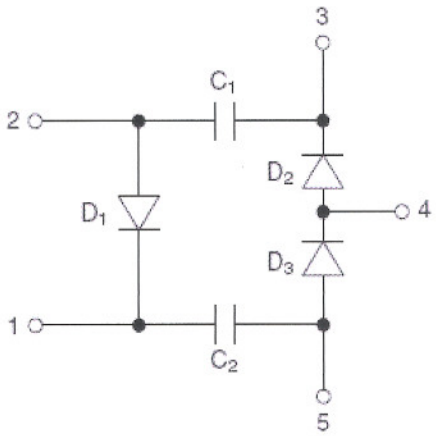

Figure 7: SPD and its elements

As it can be seen in Figure 1, a sample signal from output of the VCO will be compared with the harmonic of the reference and an error signal should be sent to the VCO after passing through a low pass filter. As the low pass filter bandwidth is low enough with respect to the difference between the frequency lock point and the free running frequency of the VCO, the error signal will not pass through the filter and the loop may not lock. Here a ramp generator circuit is vital [8]. Using this circuit and analysis of the loop for the stability, one can find the amount of different elements. Here after designing a 65 degree phase margin was achieved. The output of the PLDRO is an 11 GHz signal with phase-noise -100 dBc/Hz@10 kHz offset. A view of the PLDRO can be seen in Figure 8.

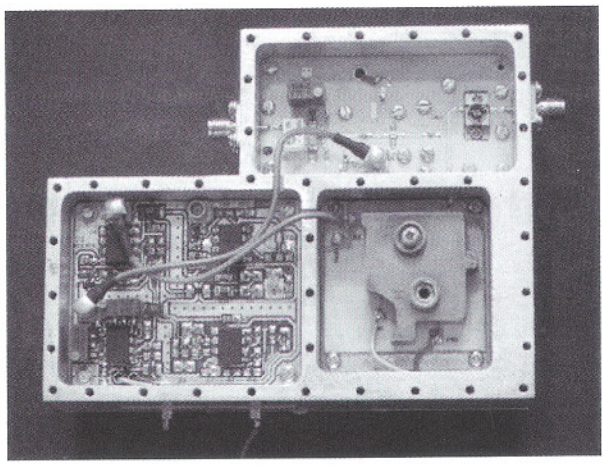

Figure 8: A view of the PLDRO

3. L-band synthesizer

For designing this synthesizer the commercial IC's were utilized. PE3340 from Peregrine Company as synthesizer IC and ROS-2150 from Mini-circuits Company were used with an active second order-second type loop. The step-size of the frequency synthesizer is 1.25MHz and the phase-noise @ 10 kHz offset is -95dBc/Hz. A view of the synthesizer is shown in Figure 9.

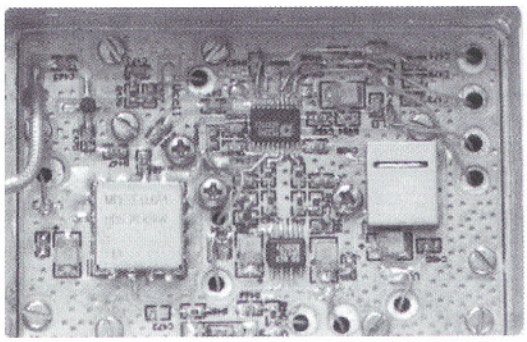

Figure 9: A view of L-band synthesizer

4. Other parts of the synthesizer

According to figure 1 an L-band synthesized signal will be mixed with a stable 11 GHz signal from the PLDRO. This mixed signal will be doubled after filtering and will generate the desired signal at the output with the phase-noise -88dBc/Hz @ 10 kHz

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offset. A figure of the box contains the L-band synthesizer and mixers and frequency doubler is shown in Figure 10.

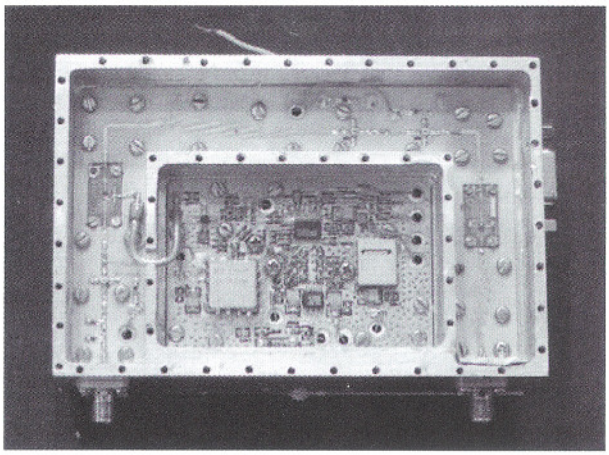

Figure 10 : a view of the box contains L-band synthesizer and other elements

5. Conclusion

An 18 GHz frequency synthesizer with a low phase noise and low step size was analyzed, designed and implemented. Using a mixing method, a highly stable signal with a low phase noise from PLDRO was mixed with and L-band synthesizer and doubled to form an 18 GHz signal.

6. Acknowledgement

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