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An 11-switch multilevel inverter with a modified space vector modulation

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Abstract: This paper proposes a new 3-phase multilevel inverter that is able to generate 7 levels in line-to-line voltage with only 11 switches. The inverter is formed from the 6-switch conventional full-bridge topology with the addition of 5 bidirectional switches in which 2 of them are shared among the three phases. By doing so, the number of power switches can be minimized, thus reducing the complexity in generating and controlling PWM signals. A novel voltage control scheme based on space vector modulation is developed by introducing a virtual vector in every sector of the vector hexagon. This is to overcome the difficulty in decomposing the reference vector in some parts of each sector. To evaluate the performance of the inverter and the effectiveness of the modulation technique in real time, a hardware prototype is constructed and the algorithm is implemented on a TMS320F2812 DSP. From the experimental results the optimum operating range of the inverter is determined to achieve the best output voltage possible with respect to quality and amplitude.

Key words: Digital signal processor, multilevel inverter, space vector modulation, virtual vector

1. Introduction

The obvious drawbacks of conventional 2-level, full-bridge inverters have paved the way for multilevel inverters. Multilevel inverters are able to produce near-sinusoidal voltage waveforms that can provide high voltage capability and reduced harmonic content. These characteristics are preferable in many medium and high-power applications. For example, in motor drives, the near-sinusoidal voltage waveforms minimize current distortion, leading to improved motor efficiency and the disappearance of vibrating torque. In addition, the low dv/dt stress prevents motor insulation breakdown.

In general, multilevel inverters can be categorized into 3 major types: the diode-clamped type [1], the capacitor-clamped type [2], and the cascaded H-bridge cells type [3]. The development of innovative topologies have flourished of late in response to several issues related to circuit complexity, total cost, efficiency, and output quality. The asymmetric cascaded H-bridge multilevel inverter is an example of those topologies. It is built by supplying unequal DC voltage amplitudes at each stage of the H-bridge cells [4,5]. In a mixed-level topology the normal H-bridge cell in a cascaded multilevel inverter is simply replaced by other cell types such as the diode-clamped-type cell [6,7]. In another topology, known as multistage topology, there are at least 2 stages in a cascaded multilevel inverter that are of different configurations, such as by combining the 3-phase 2-level full-bridge inverter as the main stage, with H-bridge cells at each arm as the secondary stage [8,9]. To control these inverters, both high and low switching frequency approaches have been applied. For instance, multicarrier

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PWM strategy [10], space vector modulation [11], and carrier-based space vector modulation [12] fall under high switching frequency approaches, while voltage vector approximation [13] and selected harmonic elimination [14] are examples of low switching frequency methods.

Another topology that has gained attention in recent years is the modified full-bridge topology, which is employed to increase the number of levels in voltage waveforms. This topology utilizes bidirectional switches, which in turn significantly reduce the number of switches used as reported in [15]. Here, a single-phase 5-level modified H-bridge structure is introduced by integrating the conventional H-bridge cell with a bidirectional switch as an auxiliary circuit to generate 5 levels in the voltage waveforms. The strong trait offered by this inverter makes the implementation in a grid-connected PV system possible, as presented in [16]. In [17], by inserting only one additional bidirectional switch in the topology, a 7-level waveform can be obtained. Using the modified H-bridge cell proposed in [15], a 3-phase structure is then developed for further investigation [18]. Another 3-phase configuration combines the 3-phase, 2-level inverter with 3 bidirectional switches to gain 5-level line-to-line voltage waveforms at the output [19].

Owing to the superior advantage of this inverter structure in easing the complexity faced in multilevel inverters via a reduction of the number of switches used, the current paper proposes a 3-phase 11-switch multilevel inverter based on the modified full-bridge configuration that is able to produce 7-level line-to-line output voltage waveforms. Section 2 provides the details of the proposed topology regarding its operational principles at a fundamental frequency. A novel space vector modulation strategy with the application of virtual vectors is covered in Section 3. Section 4 presents the power loss evaluation and related discussion. Verification of the inverter's performance by simulation and experiment is discussed in Section 5 and conclusions are drawn in Section 6.

2. The proposed topology

Figure 1 shows the proposed circuit topology consisting of an auxiliary circuit constructed from 5 bidirectional switches and a 6-switch full-bridge configuration. The line-to-line output voltage waveform is formed from 7 levels of the following amplitudes: $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, V_{dc}, $2V_{dc}$, $3V_{dc}$, and 0. For operation at the fundamental frequency in order to obtain stepped waveforms in the line-to-line output voltages, 18 operational modes are defined within a period in order to achieve 3-phase voltages at the load. Table 1 presents the description of the 18 modes and the status of their corresponding switches.

From Table 1 it can be observed that if the output voltages operate at fundamental frequency f, then Q_{A1}, Q_{A2}, Q_{B1}, Q_{B2}, Q_{C1}, and Q_{C2} also operate at the same frequency f; Q_{A3}, Q_{B3}, and Q_{C3} operate at frequency $2f$, and Q_X and Q_Y operate at frequency $3f$. It can also be seen that Q_{A1}, Q_{A2}, and Q_{A3} are exclusively used for phase A; Q_{B1}, Q_{B2}, and Q_{B3} are utilized for phase B; and Q_{C1}, Q_{C2}, and Q_{C3} are utilized for phase C. However, in the case of Q_X and Q_Y, both are shared among the three phases. This unique feature offered by the proposed topology further helps in reducing the number of switches used, thus greatly simplifying the circuit complexity. In fact, the proposed topology offers the minimum number of switches, namely 11 switches, as compared with the 3 well-known topologies that generate the same number of output voltage levels with 18 switches—a record of 38.89% less in terms of the total number of switches employed.

3. Modified space vector modulation

A major concern for the proposed inverter to operate at a fundamental frequency is its low order harmonics: the 7 voltage levels at the line-to-line output voltage have high amplitudes of low order harmonics. Therefore,

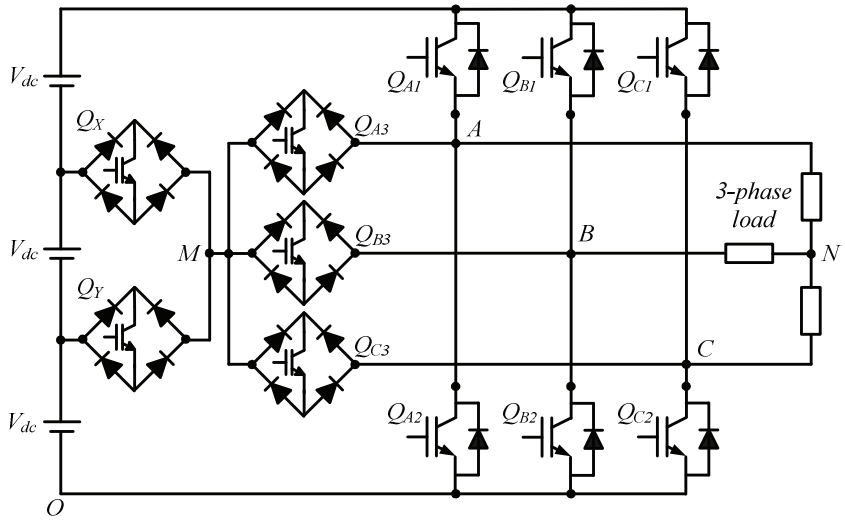


Figure 1. The proposed multilevel inverter circuit topology.

Table 1. Switching sequence of the proposed inverter.

Mode	Active switches											V_{AB}	V_{BC}	V_{CA}
	Q_{A1}	Q_{A2}	Q_{B1}	Q_{B2}	Q_{C1}	Q_{C2}	Q_{A3}	Q_{B3}	Q_{C3}	Q_X	Q_Y			
1		√		√	√							0	$-3V_{dc}$	$3V_{dc}$
2				√	√		√				√	V_{dc}	$-3V_{dc}$	$2V_{dc}$
3				√	√		√			√		$2V_{dc}$	$-3V_{dc}$	V_{dc}
4	√			√	√							$3V_{dc}$	$-3V_{dc}$	0
5	√			√					√	√		$3V_{dc}$	$-2V_{dc}$	$-V_{dc}$
6	√			√					√		√	$3V_{dc}$	$-V_{dc}$	$-2V_{dc}$
7	√			√		√						$3V_{dc}$	0	$-3V_{dc}$
8	√					√		√			√	$2V_{dc}$	V_{dc}	$-3V_{dc}$
9	√					√		√		√		V_{dc}	$2V_{dc}$	$-3V_{dc}$
10	√		√			√						0	$3V_{dc}$	$-3V_{dc}$
11			√			√	√			√		$-V_{dc}$	$3V_{dc}$	$-2V_{dc}$
12			√			√	√				√	$-2V_{dc}$	$3V_{dc}$	$-V_{dc}$
13		√	√			√						$-3V_{dc}$	$3V_{dc}$	0
14		√	√						√		√	$-3V_{dc}$	$2V_{dc}$	V_{dc}
15		√	√						√	√		$-3V_{dc}$	V_{dc}	$2V_{dc}$
16		√	√		√							$-3V_{dc}$	0	$3V_{dc}$
17		√			√			√		√		$-2V_{dc}$	$-V_{dc}$	$3V_{dc}$
18		√			√			√			√	$-V_{dc}$	$-2V_{dc}$	$3V_{dc}$

a novel PWM modulation technique based on space vector modulation is developed to suit the uniqueness of the proposed inverter. Table 2 summarizes 4 switching states that can be derived based on Figure 1. *State 0* results in $V_{JO} = 0$ and *State 1* leads to $V_{JO} = V_{dc}$, while *State 2* and *State 3* refer to $V_{JO} = 2V_{dc}$ and $V_{JO} = 3V_{dc}$, respectively, where J is the phase identity. Considering only one phase, say phase A, *State 0* is achieved when only Q_{A2} is turned on, *State 1* appears when Q_{A3} and Q_Y are active, and *State 2* is obtained when Q_X replaces Q_Y as the active switch together with Q_{A3}. The activation of Q_{A1} alone results in *State 3*. The same goes for phases B and C, too.

With respect to the three arms, 46 possible switching state combinations can be created in the form of $S_A S_B S_C$ in which S_A denotes the switching state of phase A, S_B for phase B, and S_C for phase C. Based on these combinations, the following equations are derived to represent the line-to-line and phase voltages:

Table 2. Definition of switching states.

Switching states (S_J)	Status of switch					V_{JO}
	Q_{J1}	Q_{J2}	Q_{J3}	Q_X	Q_Y	
0	Off	**On**	Off	Off	Off	0
1	Off	Off	**On**	Off	**On**	V_{dc}
2	Off	Off	**On**	**On**	Off	$2V_{dc}$
3	**On**	Off	Off	Off	**Off**	$3V_{dc}$

J – A, B, C.

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = V_{dc} \begin{bmatrix} S_A - S_B \\ S_B - S_C \\ S_C - S_A \end{bmatrix}, \tag{1}$$

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2S_A - S_B - S_C \\ 2S_B - S_A - S_C \\ 2S_C - S_A - S_B \end{bmatrix}. \tag{2}$$

By applying Park's transformation in Eq. (3) below [20], the voltage vectors can be obtained:

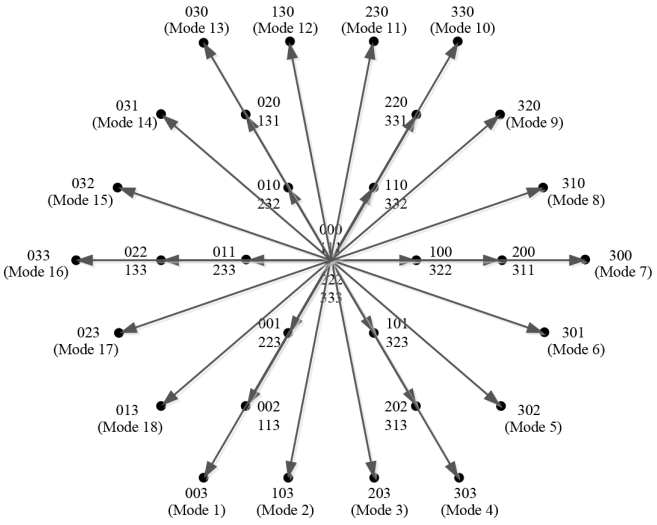
$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix}. \tag{3}$$

It should be noted that in this work, Eq. (3) does not include a coefficient of (2/3) or ($\sqrt{2/3}$) to be multiplied at the right-hand side of the equation as used in some Park's transformation representations.

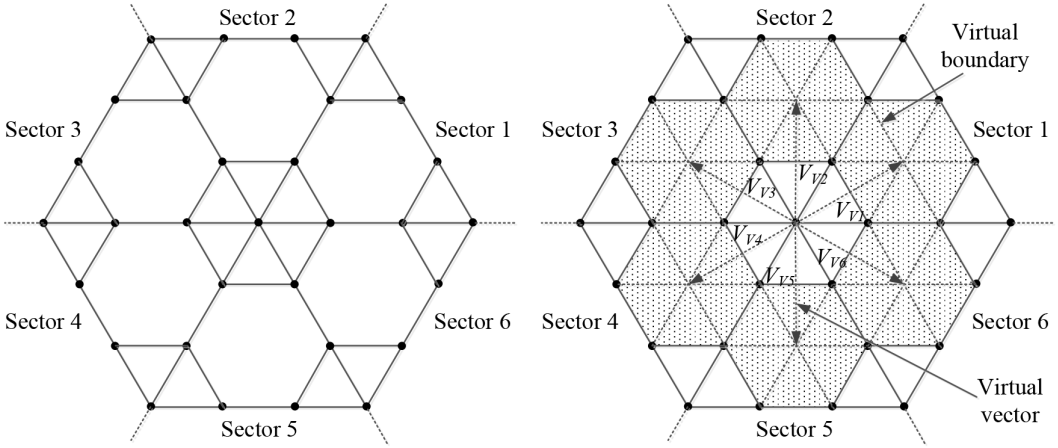
The generation of voltage vectors takes into account that both Q_X and Q_Y cannot be active at the same time as this leads to a short circuit across the voltage supply. Hence, 31 voltage vectors can be created from Eq. (3). Figures 2a and 2b portray the voltage vectors on a $d-q$ plane and the hexagon resulted from the vectors. In Figure 2a the 18 modes of operation that generate the stepped waveforms as described in Section 2 are located at the outermost voltage vectors. As seen in Figure 2b, the vector hexagon is different from the normal hexagon for a multilevel inverter generating 7-level line-to-line voltages. The condition imposed in producing the voltage vectors as mentioned above causes the elimination of 6 vectors of magnitude $\sqrt{3}V_{dc}$. As a result, each sector comprises a hexagon and 3 equilateral triangles as opposed to 9 triangles in a normal sector. A problem arises when decomposing the reference vector in the hexagon within the sector. The 6 nearest vectors that form the hexagon have to be considered in order to represent the reference vector. This contributes to complications in computing the switching time of each of the 6 vectors. To avoid this difficulty, a novel modulation technique is developed with the introduction of 6 virtual vectors so that the hexagon within the sector can be divided into 6 virtual triangles as shown in Figure 2c.

Each of the virtual vectors (V_{V1}, V_{V2}, V_{V3}, V_{V4}, V_{V5}, and V_{V6}) has a magnitude of $\sqrt{3}V_{dc}$ and is positioned at the center of each hexagon. With the presence of the virtual triangles as marked by the shaded region in Figure 2c, any given reference vector can be decomposed with much ease whereby only 2 nearest vectors are considered. Hence, to calculate the switching time of the 2 vectors, the following apply:

$$T_{1,d} = \left[\frac{V_{ref,d} - V_{2,d}}{V_{1,d} - V_{2,d}} \right] T_S, \tag{4}$$



(a) Voltage vectors



(b) Original vector hexagon (c) Modified vector hexagon with virtual vectors

Figure 2. Voltage vectors and the resulting hexagon: (a) voltage vectors; (b) original vector hexagon; (c) modified vector hexagon with virtual vectors.

$$T_{2,d} = T_S - T_{1,d}, \tag{5}$$

$$T_{2,q} = \left[\frac{V_{ref,q} - V_{2,q}}{V_{1,q} - V_{2,q}}\right] T_S, \tag{6}$$

$$T_{1,q} = T_S - T_{2,q}. \tag{7}$$

Here, $V_{1,d}$ and $V_{2,d}$ are the d-components of the 2 nearest vectors, $V_{1,q}$ and $V_{2,q}$ are the q-components, $T_{1,d}$ and $T_{2,d}$ are the switching times calculated using the d-components of the vectors, $T_{1,q}$ and $T_{2,q}$ are the switching times calculated using the q-components of the vectors, and T_s is the sampling time. To obtain T_1

and T_2, the average is calculated below:

$$T_1 = \frac{(T_{1,d} + T_{1,q})}{2}, \tag{8}$$

$$T_2 = \frac{(T_{2,d} + T_{2,q})}{2}. \tag{9}$$

Eqs. (8) and (9) are true as long as Eqs. (4) and (6) do not become infinity. If Eq. (4) becomes infinity, then $T_1 = T_{1,q}$ and $T_2 = T_{2,q}$. If Eq. (6) results in infinity, then $T_1 = T_{1,d}$ and $T_2 = T_{2,d}$. Note that for cases whereby the reference vector lies within the blank triangles in Figure 2c, the 3 nearest vectors are taken into consideration as in the conventional space vector modulation concept. The switching time of each vector is determined by solving the following equations:

$$V_{1,d}T_1 + V_{2,d}T_2 + V_{3,d}T_3 = V_{ref,d}T_S, \tag{10}$$

$$V_{1,q}T_1 + V_{2,q}T_2 + V_{3,q}T_3 = V_{ref,q}T_S, \tag{11}$$

$$T_1 + T_2 + T_3 = T_S, \tag{12}$$

where $V_{3,d}$ is the d-component of the third nearest vector, $V_{3,q}$ is the q-component of the same vector, and T_3 is the corresponding switching time for this vector.

4. Power loss evaluation

An estimation of power losses can be made by basing the analysis on the characteristic curves, usually found in the datasheets of individual power devices. Here, only conduction and switching losses are considered; the off-state loss is so small that it can be neglected [21]. Mathematical equations that reflect the curves can be derived from the relevant characteristic curves presented in the datasheet [22]. An equation that relates the voltage drop across the device and the conducted current is used to calculate the conduction loss. As for switching loss that is due to turn-on and turn-off of the switching device, the energy-loss equation is applied for the loss estimation. The diode switching loss that results from the reverse recovery process is approximated using reverse recovery time and reverse recovery current equations.

In this analysis, the power switching devices selected are the IGBT modules IRG4PC40UDPbF. The diodes used to construct the bidirectional switches are assumed to have the same characteristics as the free-wheeling diodes in the IGBT modules. From the datasheet the abovementioned equations are obtained and employed to build the mathematical models that can represent the conduction and switching losses as given in the following:

$$P_{condS} = \frac{1}{T_p}\int_0^{T_p} (3.141e^{0.003496i(t)} - 2.296e^{-0.01392i(t)})i(t)dt, \tag{13}$$

$$P_{condD} = \frac{1}{T_p}\int_0^{T_p} \left(1.396e^{0.009157i(t)} - 0.5844e^{-0.1733i(t)}\right) i\,(t)\,dt, \tag{14}$$

$$E_{swS} = 15.62e^{0.009769i(t)} - 15.62e^{0.009764i(t)}, \tag{15}$$

$$E_{swD} = \left[16.2e^{0.003252i(t)} - 10.4e^{-0.076497i(t)} - 1.815e^{-0.076441i(t)} + 1.166e^{-0.15619i(t)}\right] \times 10^{-6}, \tag{16}$$

$$P_{swS} = \frac{1}{T_p}\sum E_{swS}, \tag{17}$$

$$P_{swD} = \frac{1}{T_p} \sum E_{swD}, \tag{18}$$

$$P_{loss} = P_{condS} + P_{condD} + P_{swS} + P_{swD}, \tag{19}$$

where T_p is the period for one cycle, P_{condS} is the IGBT conduction power loss, P_{condD} is diode conduction power loss, E_{swS} is the IGBT switching energy loss, E_{swD} is the diode switching energy loss, P_{swS} is the IGBT switching power loss, P_{swD} is the diode switching power loss, and P_{loss} is the total power loss.

The analysis is conducted at a switching frequency of 4.6 kHz using MATLAB/Simulink software. The inverter is supplied with a 150-V DC voltage ($3V_{dc}$ equals 150 V) and connected to a Y-connected load of 30.5 Ω per phase. For comparison purposes the power loss assessment of the equivalent diode-clamped inverter is also carried out with the application of the conventional space vector modulation at the same switching frequency. Figure 3 shows the power losses generated by both inverters at a reference voltage amplitude of 80%. The proposed inverter records a total power loss of 17.17% less than that of the diode-clamped inverter. Most of the losses are contributed by the conduction loss in the IGBTs and diodes. In the proposed inverter 59.02% of the total power loss is due to the IGBT conduction loss and 37.14% comes from the diode conduction loss. As for the diode-clamped inverter, IGBT and diode conduction losses contribute to 86.36% and 6.41% of the total power loss respectively. The smaller number of IGBTs used in the proposed inverter clearly plays a significant role in reducing the total power loss despite the increase in the number of diodes. If only conduction and switching losses are considered in estimating efficiency, then the proposed inverter has higher efficiency (95.65%) as compared with the efficiency of the diode-clamped inverter (94.76%).

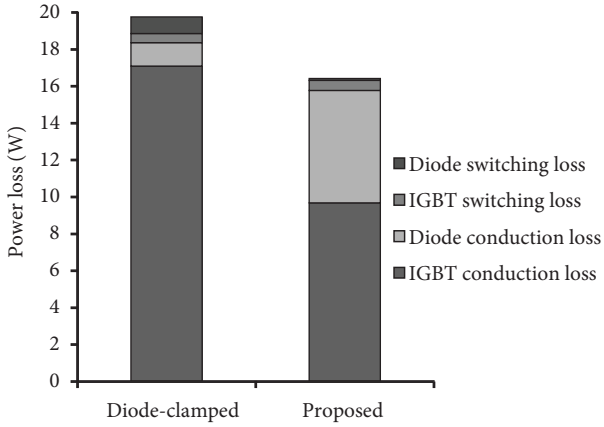


Figure 3. Power loss comparison.

5. Results verification

5.1. Simulation

Computer simulation is carried out as the first step to verify that the proposed inverter can function as expected according to the PWM principles presented above. For this purpose MATLAB/Simulink software is used. The input DC voltage is set to generate 150 V and a three-phase Y-connected load of 30.5 Ω and 68 mH per phase is used. The modified space vector modulation is employed with a switching frequency of 4.6 kHz to generate the PWM switching signals. To have a meaningful comparative analysis, the conventional space vector modulation technique with the same switching frequency is also simulated for the equivalent diode-clamped inverter.

Figure 4 provides the simulation results. Figure 4a shows the line-to-line voltage, which verifies the presence of 7 voltage levels; in Figure 4b the corresponding harmonic spectrum is given. These results are obtained at a reference voltage amplitude of 80% from the maximum value. Results for the case of 50% reference voltage amplitude are displayed in Figures 4c and 4d, while those that represent the case of 20% reference voltage amplitude are depicted in Figures 4e and 4f. In order to evaluate the performance of the proposed inverter with the novel modulation technique as opposed to that of the diode-clamped counterpart with conventional space vector modulation, both total harmonic distortion (THD) and the fundamental voltage amplitude are studied and the results are displayed in Figures 5a and 5b, respectively.

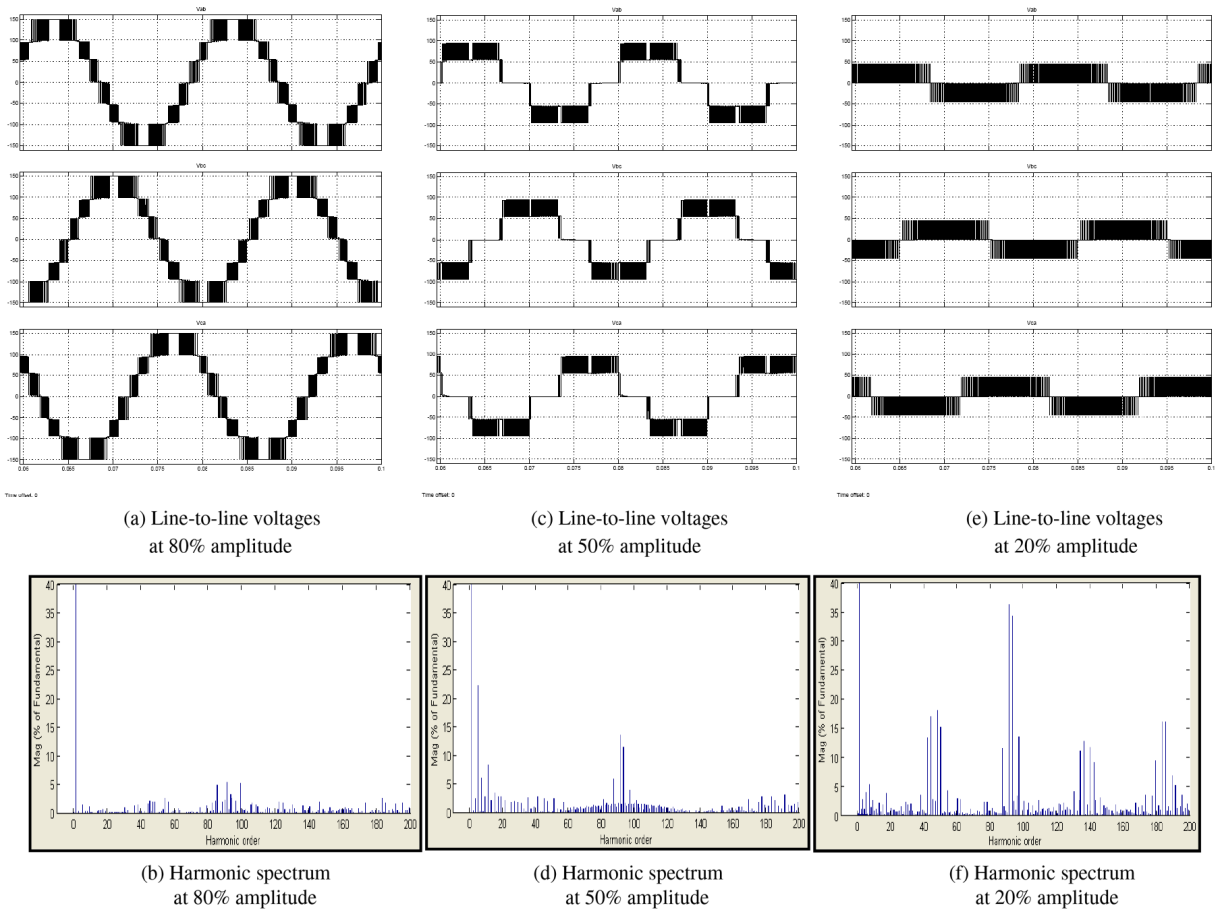
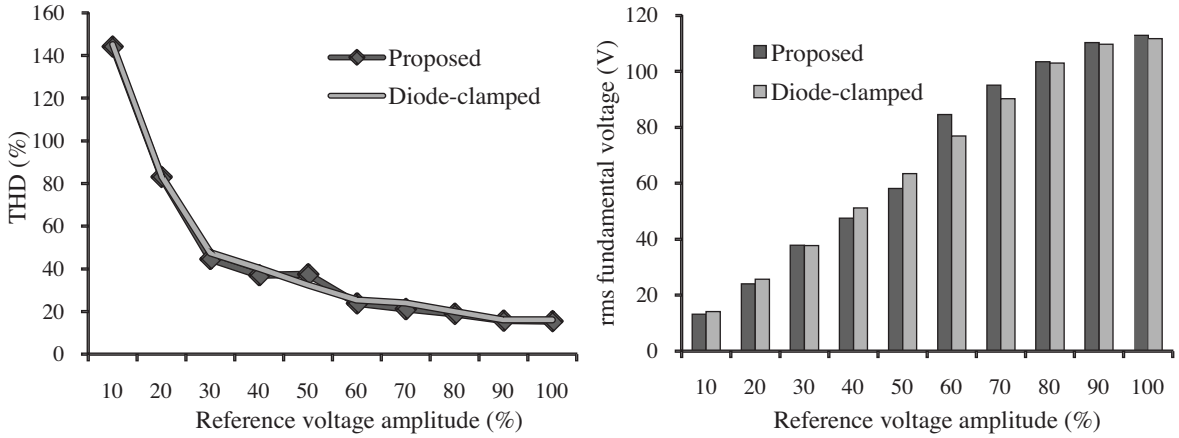


Figure 4. Simulation results: (a) line-to-line voltages at 80% amplitude; (b) harmonic spectrum at 80% amplitude; (c) line-to-line voltages at 50% amplitude; (d) harmonic spectrum at 50% amplitude; (e) line-to-line voltages at 20% amplitude; (f) harmonic spectrum at 20% amplitude.

The THD results reflect a close agreement between the 2 inverters for all reference voltage amplitudes except at 50% amplitude, where the absence of the 6 voltage vectors stated earlier causes an increase in THD of 15.86%. In terms of the fundamental voltage amplitude, however, it appears that both inverters portray an upward trend as the reference voltage amplitude increases. It is important to note that the proposed inverter records higher fundamental voltage values for reference voltage amplitudes bigger than 50%, thus proving another advantageous trait of the proposed inverter.



(a) Line-to-line THD comparison

(b) Line-to-line fundamental voltage comparison

Figure 5. Performance comparison between the proposed inverter and the equivalent diode-clamped inverter: (a) line-to-line THD comparison; (b) line-to-line fundamental voltage comparison.

5.2. Experiment

Practical experiments are carried out as the next step to prove that the proposed inverter can be implemented in a real-time environment. The inverter is built using 600-V IGBTs as power switches, gate drive circuits, and a dead band generation circuit. Each bidirectional switch consists of 1 IGBT and four 30-A, 1200-V hyperfast diodes. A resistive load of 30.5 Ω, coupled with a 68-mH inductor per phase with Y connection, is used. The modified space vector modulation algorithm is implemented on a DSP controller board eZdsp F2812. The fixed-point TMS320F2812 DSP processor executes the algorithm at a sampling frequency of 4.6 kHz. Figures 6 and 7 show the experimental setup and its block diagram.

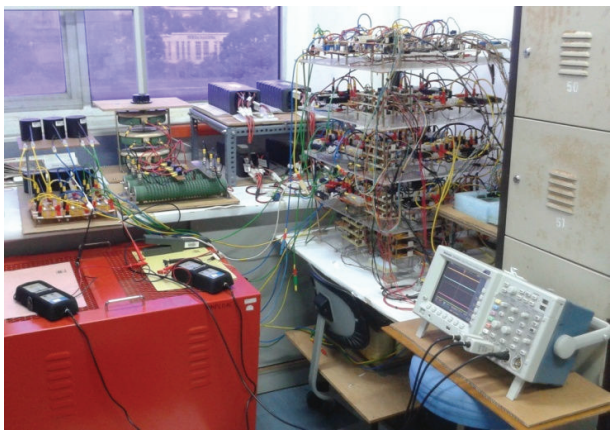


Figure 6. Experimental setup.

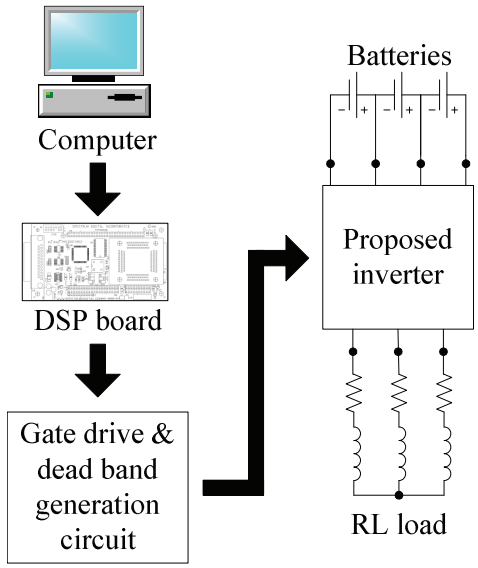
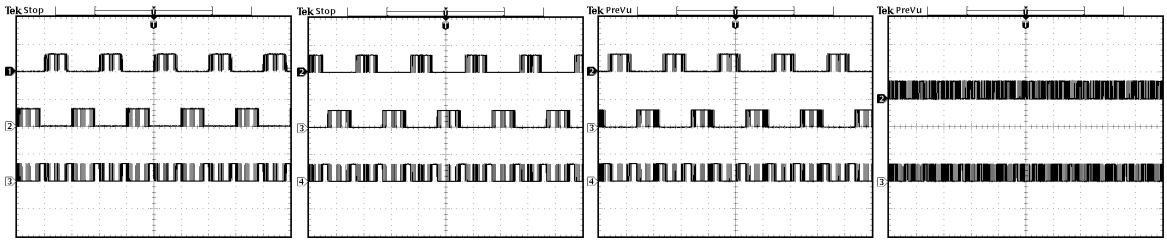


Figure 7. Block diagram of the experimental setup.

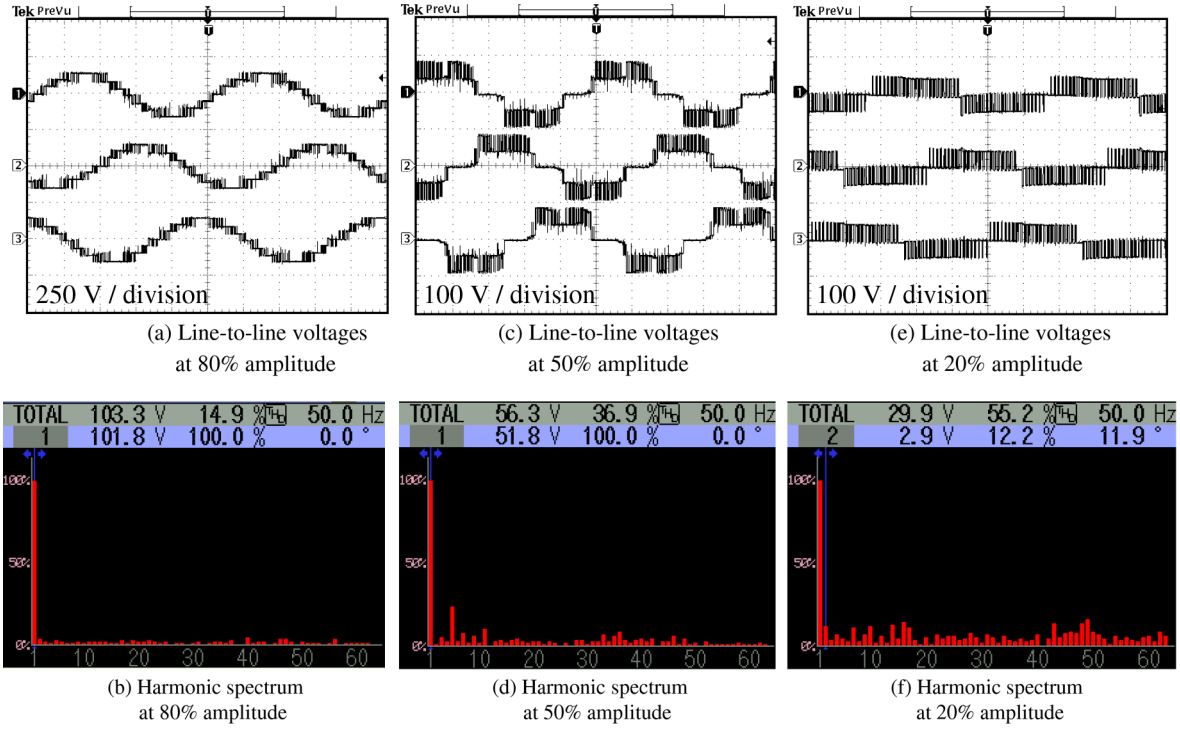
Figure 8 displays the gating pulses for all switches at 80% reference voltage amplitude whereby the inverter is able to generate 7-level line-to-line voltages. Figure 9 is used to investigate the impact of variation of

the reference voltage amplitude on the inverter's output voltage magnitude and quality. It can be seen that as the reference voltage amplitude increases, the number of line-to-line voltage levels also rises. Figure 9a shows the representation of the 7-level waveform obtained at 80% amplitude and the corresponding harmonic spectrum is provided in Figure 9b. A 5-level waveform and its harmonic spectrum, both measured at 50% amplitude, are displayed in Figures 9c and 9d respectively. For a 3-level waveform and the harmonic spectrum captured at 20% amplitude, Figures 9e and 9f are given respectively.



Q_{A1}, Q_{A2} and Q_{A3} Q_{B1}, Q_{B2} and Q_{B3} Q_{C1}, Q_{C2} and Q_{C3} Q_X and Q_Y

Figure 8. Gating signals at 80% reference voltage amplitude.



(a) Line-to-line voltages at 80% amplitude

(c) Line-to-line voltages at 50% amplitude

(e) Line-to-line voltages at 20% amplitude

(b) Harmonic spectrum at 80% amplitude

(d) Harmonic spectrum at 50% amplitude

(f) Harmonic spectrum at 20% amplitude

Figure 9. Experimental results: (a) line-to-line voltages at 80% amplitude; (b) harmonic spectrum at 80% amplitude; (c) line-to-line voltages at 50% amplitude; (d) harmonic spectrum at 50% amplitude; (e) line-to-line voltages at 20% amplitude; (f) harmonic spectrum at 20% amplitude.

Harmonics analysis is performed to further study the effect on the THD for the 3-level, 5-level, and 7-level waveforms. As expected, a better harmonic spectrum is achieved as reference voltage amplitude increases. THD also decreases from 61.7% at 20% amplitude to 36.9% at 50% amplitude. Further reduction is seen at 80% amplitude with a measurement of 14.9% THD. At 20% amplitude, 9 harmonic components record magnitudes

higher than 10.0% of the fundamental component, with the 49th harmonic being the most significant, indicating 15.97%. Although only 2 harmonic components reach magnitudes higher than 10.0% at 50% amplitude, the 5th (23.5%) and the 11th (10.0%) harmonics, the fact that those dominant harmonics are of low order contributes to the significant increase in the THD. For 80% amplitude all harmonic components are of magnitudes below 5%, with the highest being 4.2% at the 40th harmonic.

While THD decreases, the rms voltage magnitude certainly increases from 29.9 V at 20% amplitude to 56.3 V at 50% amplitude and 103.3 V at 80% amplitude. These experimental results are in accordance with the simulation results. Figure 10 provides the comparative details between the 2 sets of results in terms of THD and fundamental voltage magnitudes. This shows the validity of the practical feasibility of the proposed inverter with the modified space vector modulation technique.

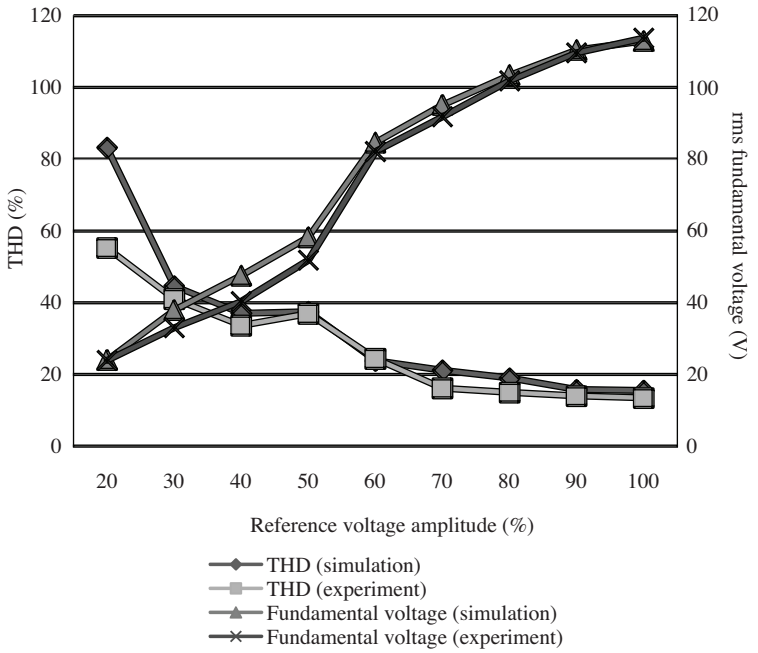


Figure 10. Line-to-line THD and fundamental voltage comparison between simulation and experiment.

6. Conclusion

In this paper, a new multilevel inverter generating 7-level line-to-line output voltages that uses the minimum number of power switches (only 11 switches as opposed to other equivalent topologies) has been presented. The significant reduction in the number of switches is achieved by sharing two bidirectional switches (Q_X and Q_Y) among the three phases, thus greatly reducing complexity. Although the number of diodes employed increases through the use of bidirectional switches, the fact that diodes are much cheaper than power switches such as IGBTs contributes to a reduction in the overall cost. Less overall heat dissipation can still be achieved with the proposed inverter due to the lower number of IGBTs even though the diode's heat loss is usually higher than that of the IGBTs. Despite the elimination of $\sqrt{3}V_{dc}$ voltage vectors, voltage control can still be effectively achieved using the modified space vector modulation technique. From the results obtained, the proposed inverter shows similar performance to that of the equivalent diode-clamped inverter. In fact, for high reference voltage amplitudes the proposed inverter slightly outperforms the benchmark inverter. To fully exploit the advantages of the 7-level output that offers a better harmonic spectrum and a higher voltage magnitude, the inverter has

to operate within the optimum range of the reference voltage amplitude, i.e. higher than 54.2%. The fact that two bidirectional switches are shared among the three phases makes the proposed topology unique in its kind.

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