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Designing a new high gain CMOS amplifier towards a 17.22 MHz MEMS based Si oscillator for a cost effective clock generator IC

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Abstract: A novel sustaining amplifier is designed and characterized for a Si-based MEMS resonator, in implementing a reference oscillator in 180 nm CMOS process. A two port electrical model of the MEMS resonator is used to compute the insertion loss (−76 dB) and phase shift (95°). Total open loop transimpedance gain is achieved as 122 dBΩ with −70° phase shift, at the resonant frequency of 17.22 MHz. This amount of gain is investigated as capable to sustain MEMS resonator's oscillation, in the realization of a cost effective, miniaturized and low power CMOS reference oscillator which oversees on application in clock generation.

Keywords: sustaining amplifier, transimpedance amplifier, MEMS, electrostatic resonator, CMOS 180 nm

Classification: Micro- or nano-electromechanical systems

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1 Introduction

In recent years, Silicon (Si) based MEMS resonators are replacing the conventional crystal resonator for tunable frequency application with a comparable thermal compensated performance [1]. CMOS MEMS based resonator also offers the avenue of single chip integration, inheriting small form factor in area with high quality factor ($Q > 40,000$) and less power consumption, which favorably penetrates the market of the timer circuit highlighting the compliance to Moore's law [2, 3, 4]. But, the high insertion loss of MEMS devices which results from their low Q and high motional resistance (up to several kΩ) [5], is the first major obstacle to overcome. In this work, a CMOS operational amplifier is designed which replenishes all the motional losses of a clamp-clamp (C-C) beam Si-MEMS resonator in realizing a single chip oscillator. In commercial applications, such oscillator can be a functional part of a phase locked loop of a voltage controlled oscillator or a very small clock generator.

2 MEMS resonator modeling

The motional losses of a C-C beam MEMS resonator [Fig. 1(a)], with an unloaded Q of 1000 are electrically modeled with a series RLC circuit equivalents [Fig. 1(b)] from its S_{21} (Forward Transmission) measurement response. From these modeled lumped values, the required gain and phase shift are estimated from its insertion loss of −76 dB with a transmission phase of 95° values [Fig. 1(c)]. Subsequently, this model is adopted to design a CMOS sustaining amplifier which makes and sustains the oscillation of the resonator by complementing Barkhausen criteria [6] and hence fulfilling the objective of this work.

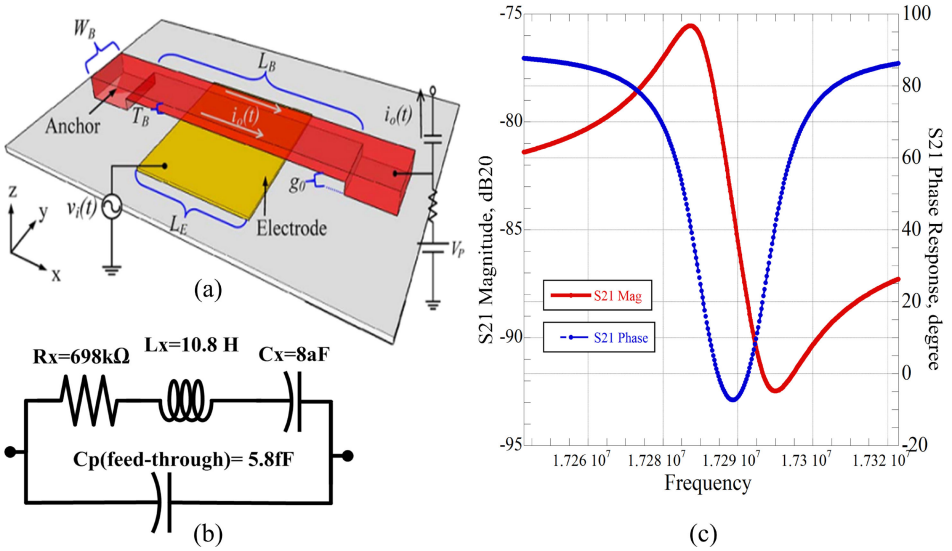

Fig. 1. (a) A 3D view of C-C beam MEMS resonator with necessary bias and signals (b) RLC equivalent model with electrically fitted lumped values of the MEMS (c) Insertion loss and phase shift response of it.

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3 Designing of sustaining amplifier

The designed integrated operational amplifier, has three different 'single ended' amplification blocks, cascaded together. The initiating block is a high gain transimpedance amplifier (TIA) which tasked to convert the MEMS capacitive current, $i_{MEMS}(t)$, as shown in Fig. 2(a), into an amplified voltage signal.

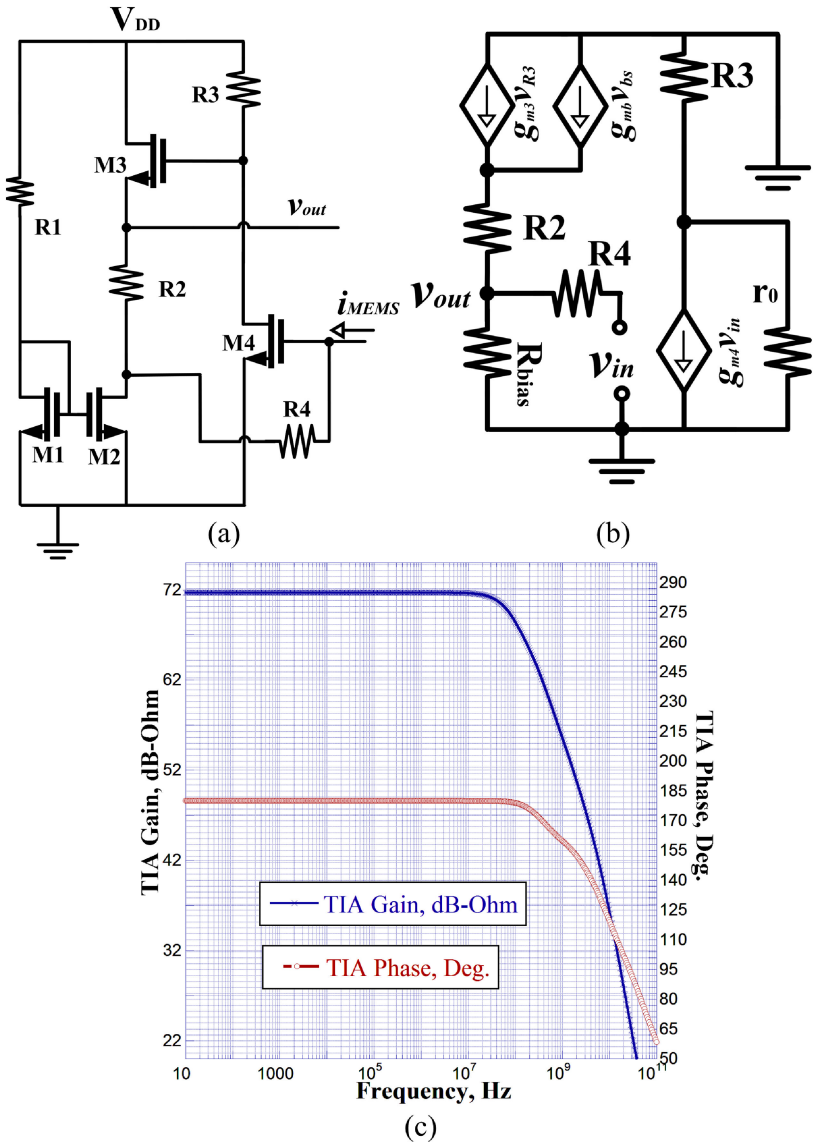

Fig. 2. (a) Schematic of transimpedance amplifier (b) Its small signal equivalent (c) TIA gain and phase response.

Fig. 2 illustrates the TIA where its core amplifying component consists the transconductance (g_m) of common source (CS) M4 and source follower M3, where the source follower isolates R3 from the loading effect of feedback resistor, R2 and R4. As long as the output impedance of source follower is kept much less than feedback resistor, the close loop gain can be regulated by R2 and R4. When the current, i_{MEMS} from MEMS is zero, the gate voltage of M4 is equal to DC value of output voltage, v_{out}. If i_{MEMS} eventually increases, most of the current will route through R4 and will be sinking through the current source. In line with this, the

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current through M3 and R2 will also be increased by which, the MEMS output current in value can be converted and sensed into a voltage drop signal across R2. But, for substantial i_{MEMS}, voltage drop across R4 will result into v_{out} dropped and the current source will approach the non-linear region as it reaches i_{MEMS}. Due to this, R4 is designed as minimum for maintaining linearity, whereas R2 is adjusted for high gain and noise performance with respect to V_{DD} and bias current. Eqs. (1) to (4) can be derived from the small signal gain analysis [Fig. 2(b)] of TIA. As seen in the bode plot of TIA [Fig. 2(c)], a flat 72 dB 'TIA' gain is achieved with a 182° phase over the intended bandwidth of 17.22 MHz resonator.

$$V_{in} - V_{out} = I_{MEMS}R_4 + I_{R2}R_2 \tag{1}$$

$$\Rightarrow V_{out}\left(\frac{1}{-g_{m3}R_3} - 1\right) = I_{MEMS}(R_4 - R_2) + I_{R3}R_2 \tag{2}$$

$$\Rightarrow V_{out} = I_{MEMS}\left(\frac{(-g_{m3}R_3)(R_4 - R_2)}{1 + g_{m3}R_3}\right) + I_{R3}\left(\frac{(-g_{m3}R_3)(R_2)}{1 + g_{m3}R_3}\right) \tag{3}$$

By considering larger M3, the close loop transimpedance gain (R_T) becomes the sum of the adjustable resistances in the feedback loop.

$$R_T = \frac{g_{m3}R_3}{1 + g_{m3}R_3} * (R_4 + R_2) \approx (R_4 + R_2) \tag{4}$$

In the second block of the complete amplifier [Fig. 3(a)], the gain is tuned by means of a R6-C2 'T' network in shunt-shunt feedback configuration that intro-

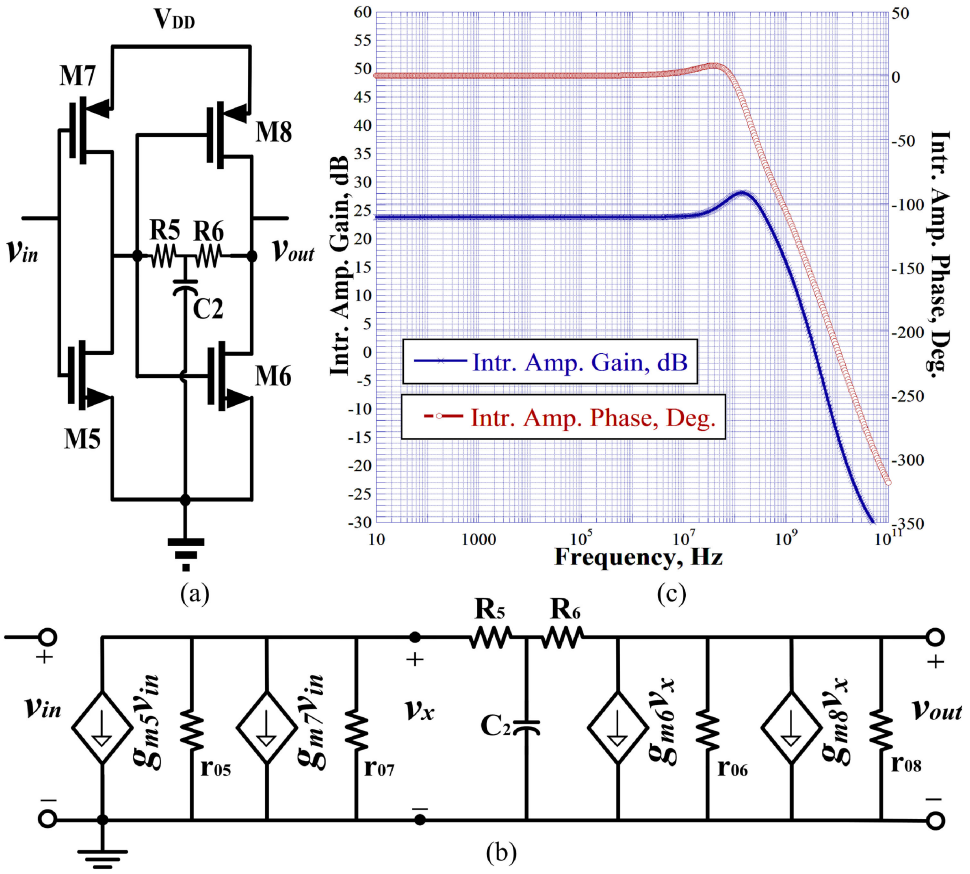

Fig. 3. (a) Intermediate voltage amplifier (b) Its small signal equivalent (c) Gain and phase response.

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duces an additional zero, which will be used in pole cancellation and would offer less input and output impedance to the next stage. Additionally, this R6-C2 will shift the poles to higher frequency, thus increasing the bandwidth. Hence, both of the gain and bandwidth can be tuned at this stage separately, which is an advantage. The gain expressions in Eqs. (5) to (6) can be derived from the circuit in Fig. 3(b) and in AC response, a 24 dB voltage gain is achieved with the intended minimal 5° phase shift over the bandwidth of interest [Fig. 3(c)].

$$\frac{v_x}{v_{in}} = (g_{m5} + g_{m7})(r_{05} \| r_{07}) \tag{5}$$

$$\frac{v_{out}}{v_{in}} = \frac{(g_{m5} + g_{m7})(r_{05} \| r_{07})(1 + s2R_5C_2)}{1 + sR_5C_2} \tag{6}$$

For the third stage [Fig. 4(a)] of this sustaining amplifier block, a cascode amplifier is designed to give the rest of the needed voltage gain and phase shift.

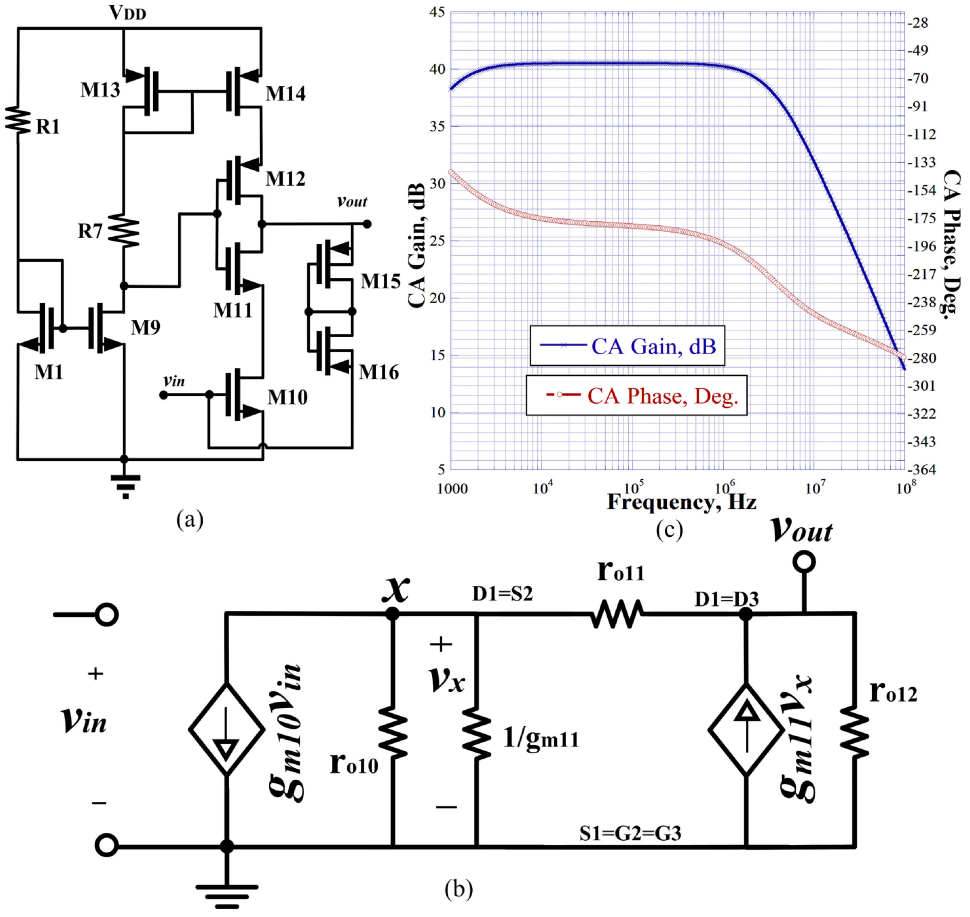

Fig. 4. (a) Cascode amplifier (b) Simplified small signal equivalent (c) Gain and phase response.

Cascode architecture is chosen for getting a high gain, a high input impedance and an extended bandwidth which is ensured by reducing Miller feedback from its CS portion. The CS amplifier consists of M10 whereas M11 is a common gate (CG) configuration. The feedback path from the output node to the gate of CS is through a high resistance (~8k8 Ω) which is implemented by M15 and M16, in PMOS pseudo-resistor configuration for biasing the CS stage (M10) where the output

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voltage signal from the previous stage [Fig. 3(a)] will be imposed on this biasing through a 500 fF decoupling capacitor. Moreover, M12 benefits in an additional gain depending on the bias of CG stage. Current source (M13, M14 and R7) and M9 ensures the necessary biasing for CG stage. Now by locating node 'x' and v_{out} in Fig. 4(b), and performing circuit analysis at these nodes, the required gain expression can be derived which is in Eq. (10). In associated bode plot [Fig. 4(c)], it is seen that, a high gain of 30 dB is achieved over the bandwidth of interest.

$$(g_{o10} + g_{o11} + g_{m11}) * v_x - g_{o11} * v_{out} = -g_{m10} * v_{in} \tag{7}$$

$$(-g_{m11} - g_{o11}) * v_x + (g_{o11} + g_{o12}) * v_{out} = 0 \tag{8}$$

The desired gain expression in Eq. (10) can be derived by solving Eqs. (7) and (8).

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m10}(g_{o11} + g_{m11})}{g_{o10}g_{o11} + g_{o10}g_{o12} + g_{o11}g_{o12} + g_{o12}g_{m11}} \tag{9}$$

$$\frac{v_{out}}{v_{in}} \cong \frac{-g_{m10}}{g_{o12}} \equiv -g_{m10} * r_{o12} \tag{10}$$

4 Results and discussion

In the bode plot [Fig. 5], a highest 135 dB-Ω gain has been achieved for the sustaining amplifier and at resonant frequency, it is 122 dB-Ω, as shown in Table I. But based on the conventional MEMS oscillator theory in F. Nabki's work in 2009 [5], at least 1.5 times of motional resistance can be targeted to set the minimum transimpedance gain in designing a CMOS sustaining amplifier. Hence, the required "Transimpedance gain" should be greater than $20\log_{10}(698\,\text{k}\Omega * 1.5)$ or, 120.39 dB-Ω.

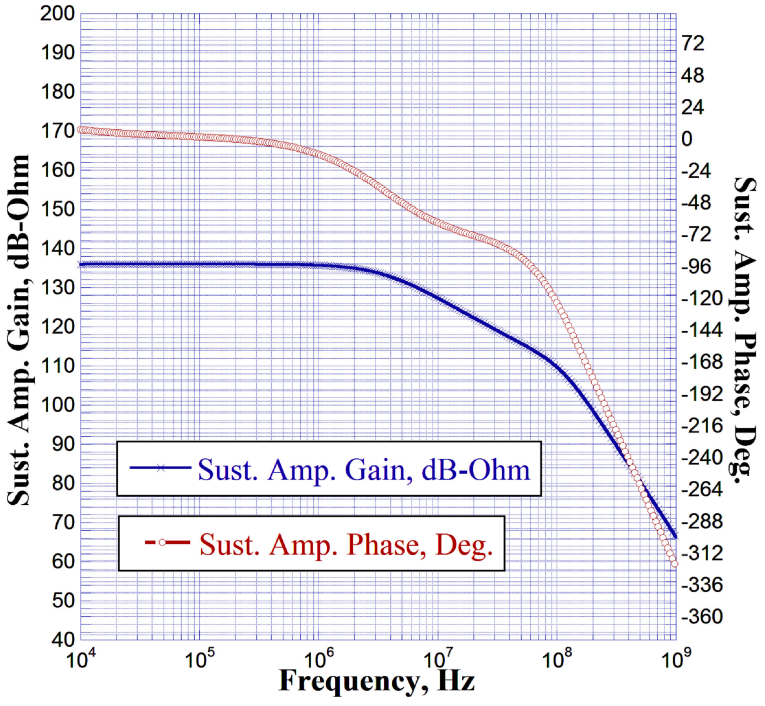

Fig. 5. Bode plot of the complete sustaining amplifier.

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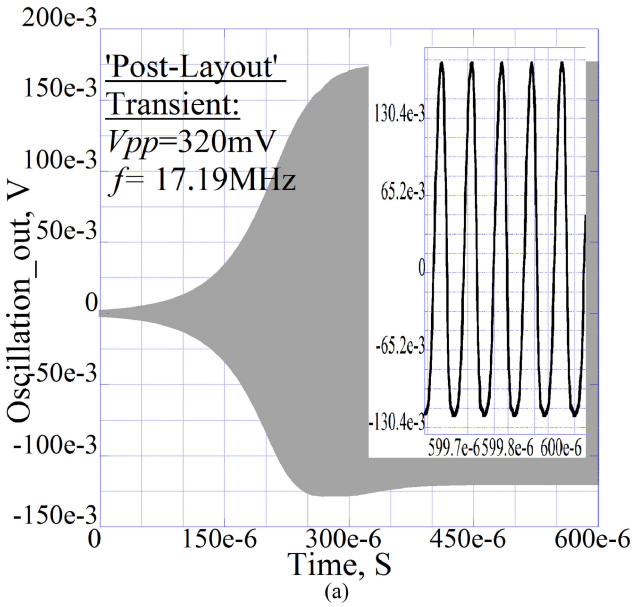
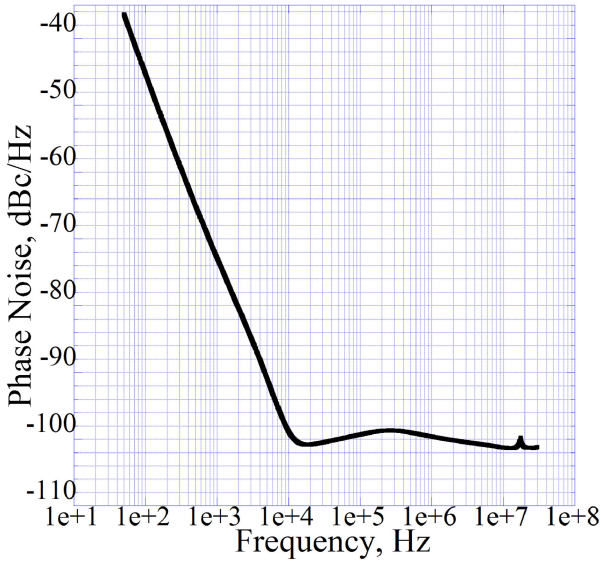
Table I. Performance summary of the sustaining amplifier at 17.22 MHz

Amplifier stages	Gain	Phase (x^0)
TIA	72 dB-Ω	182
Inter. voltage amplifier	24 dB	5
Cascode amplifier	30 dB	−255
Sustaining amplifier	122 dB-Ω	−70
Total power consumption from 1.8 V_{DC} w/o, buffer	6.24 mWatt	



(a)



(b)

Fig. 6. (a) Oscillator output transient response (b) Oscillator phase noise response.

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As shown in Table I, the total 'transimpedance' gain has been achieved as 122 dB-Ω at MEMS resonant frequency of 17.22 MHz, which fulfills the criteria highlighted above [5]. Additionally, total phase shift achieved is -70^0, which is nearly nullifying MEMS phase shift of $+95^0$ as found from S_{21} data in Fig. 1(c).

Therefore, it is evident from the simulation that, the designed CMOS amplifier is capable to sustain the desired 17.22 MHz oscillation with this MEMS resonator intact in a close loop feedback position. In Fig. 6, the 'post layout' close loop sustained oscillation has defended this where the phase noise spectrum has also fulfilled the design's applicability in a low frequency clock generator IC. Now, a low unloaded Q of such a MEMS resonator can be a limiting factor for oscillator's performance, but this can be improved by designing CMOS circuitry properly. In Table II, a performance comparison is also drawn, where the proposed oscillator has achieved a better gain and moderate phase noise with a much lower 'Q' resonator.

Table II. Comparison between different Q based MEMS oscillator works

Parameters	[3]	[5]	[6]	This work
Resonator Q	>40,000	1040	2000	1000
Amplifier Gain, dB-Ω	99	(81–112)	76	(122–135)
PN @ 10 kHz, dB_c/Hz	−130	−90	−119	−102

5 Conclusion

In this work, a 122 dB-Ω sustaining amplifier has been reported with evidence for realizing a 17.22 MHz Si-MEMS resonator based CMOS oscillator which can also be fabricated monolithically in 180 nm CMOS process to ensure a cost effective production for its dedicated application area (i.e., clock generator IC).

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