# A 0.13µm Inductively Degenerated Cascode CMOS LNA at 2.14GHz

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***Abstract*— A 130-nm CMOS low-noise amplifier (LNA) for WCDMA applications is presented. The circuit adopts an inductively degenerated cascode topology. A detailed methodology using power constraint noise optimization (PCNO) method that leads to an optimum width of the LNA is presented. A theoretical noise figure optimization using fixed power was used as a design optimization guide. This inductively degenerated cascade topology show good noise performance which it achieve a noise figure of 1.32dB while provides a forward gain, $S_{21}$ of 18.24 dB from a 1.2V voltage supply. The input reflection coefficient, $S_{11}$ is -19 dB.**

***Keywords- Cascode LNA; Inductively degenerated; Power Constraint Noise Optimization (PCNO); WCDMA***

## I. INTRODUCTION

Radio Frequency (RF) and analogue mixed-signal technologies serve the rapidly growing wireless communication market and the growing demand for larger bandwidth motivates the RF circuits to advance to higher frequencies. The current trend in RF communication system nowadays is to produce receiver that is small, cheaper and low power. The direct-conversion receiver (DCR) is a good choice because it can be integrated in a single–chip application. LNA is the backbone of RF communication receivers as it is the first gain stage in the receiver path. Its main function is to increase the input signal level, while at the same time minimizing the increment of the noise figure (NF) of the whole receiver system. In other words, an LNA is to provide enough gain to the input signal to enable the signal to tolerate the noise of the subsequent stages while contributing as little noise as possible to the signal. The LNA designed in this project is for the WCDMA application. W-CDMA is also commonly known as Universal Mobile Telecommunications System (UMTS). UMTS is the 3G standard in Europe whereas W-CDMA is the standard for 3G in Japan. Irrespective of what it is known as, W-CDMA (or UMTS) is a mobile communications technology that can cater data transmission speeds up to 2 megabits per second (Mbps). Actual speeds are lower at first due to the capacity limit on the network. WCDMA has a transmitting frequency band in the range of 1920 -1980 MHz. The received frequency band is in the range of 2110-2170 MHz. To give an overview about this paper, it will be organized as follows. Section II describes the chosen topology to be implemented in the LNA circuit which is inductively degenerated cascode LNA topology. Then, section III will explain the detail design methodology carried out and Section IV will show the result and analysis of the simulated design and discussion of LNA. Finally, Section V will conclude the research findings.

## II. CIRCUIT TOPOLOGY

Inductively degenerated cascode LNA is chosen to be implemented for WCDMA application. This topology was chosen because it is the basic topology to most of the varieties of LNA topologies presently available. It allows for maximizing gain under low power constraint and also has good input and output isolation. Good reverse isolation will improve stability and simplify input port matching [1]. The basic schematic for the mentioned topology is adopted from [1]. The simplified schematic of the proposed CMOS LNA for simultaneous noise and input matching is illustrated in Fig 1.

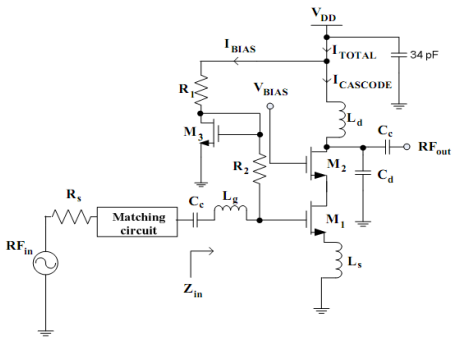


Figure 1. A typical Inductively-degenerated cascode CMOS LNA

The propose LNA is to be designed such that to comply with the WCDMA specifications whereby the LNA needs to provide a high gain of greater than 15 dB with a noise figure of lower than 2 dB and operating at low power. Its resonance frequency tuned at around 2110MHz to 22170 MHz. The input and output reflection coefficient should ideally be lesser than -10 dB. This is in order to have good input and output matching and circuit stability.

Base from circuit in Figure 1, $L_d$ and $C_d$ provides output matching. Besides this, their combination at resonance enables additional filtering to the output. In addition to these, the voltage drop across the inductor is contributed by its series resistance only and hence, this configuration is very attractive for low power design. $M_3$ and $R_1$ form a current mirror circuit with $M_1$ isolates the signal path from the biasing circuit and in this way enforces the input signal to the LNA input. The value of $R_2$ is not critical as long as it is much greater than the input impedance of the stage prior to it.

At resonance, the input resistance is to indicate that the combination of the transistor with the degeneration inductor provides input matching [2] . The impedance looking into the input is given by:

$$Z_{in} = s(L_g + L_S) + \frac{1}{(s\,C_{gs})} + \frac{g_m L_S}{C_{gs}} \quad (1)$$

where input resistance is given by:

$$R_{in} = Re\,[Z_{in}\,] = \frac{g_m L_s}{C_{gs}} \quad (2)$$

Also at this frequency,

$$\omega^2 = (L_g + L_s)C_{gs} = 1 \quad (3)$$

The gain of the LNA is given by the following equation:

$$\frac{V_{out}}{V_{in}} = \frac{-g_m s L_d}{1 - \omega^2 C_{gs}(L_g + L_s) + sL_s g_m} \quad (4)$$

And substituting (3) into (4) will give;

$$\frac{V_{out}}{V_{in}} = \frac{-g_m\, sL_d}{sL_s g_m} = \frac{-L_d}{L_s} \quad (5)$$

This equation shows that the gain is the ratio of the inductor at the drain to the inductor at the source. A higher gain can be achieved if the value of $L_d$ is set to be higher than $L_s$. However, there is a trade-off between the size of $L_d$ and the output performance of the circuit due to the series resistance of the inductor [3].

## III. LNA Design Methodology

### A. Determination of Transistor's Width

The initial stage was to determine the size of the transistor. The amplifying transistor M1's width is being determined by using the power constraint noise optimization (PCNO) method. By using PCNO techniques, there is an expression that relates the width of $M_1$ noise of the LNA [4]. The following equation in used in determining the width of $M_1$.

$$W_{opt} \approx 1.5\,(\omega_{\square}\, LC_{ox}R_s Q_{in\ opt,P_D})^{-1} \quad (6)$$

In order to understand how equation (6) was developed, the following derivations should be done. The derivation starts with Equation (6) which is the noise expression obtained from the Classical Noise Matching (CNM) [2].

$$F = F_{min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s + B_{opt})^2\right] \quad (7)$$

The purpose is to re-express Equation (7) in terms of power consumption. Once this expression is obtained, the noise should be minimized at fixed power and the corresponding transistor's width under this condition subsequently can be determined [2]. From Lee, 2004 also state that;

$$G_{opt} = \sqrt{\frac{G_U}{R_n} + G_c{}^2} = \alpha\omega_o C_{gs}\sqrt{\frac{\delta}{5\gamma}(1 - |c|^2)} \quad (8)$$

where $G_{opt}$ is the optimum conductance, $G_u$ is the conductance due to the current uncorrelated with the voltage noise generator, $e^n$ $R_n$ is the noise resistance due $e^n$.

The optimum quality factor, $Q_{opt}$, is given by the following equation:

$$Q_{opt} = \frac{1}{\omega_o C_{gs} R_{opt}} \quad (9)$$

where $R_{opt}$ is the inverse of $G_{opt}$.

$$Q_{opt} = \frac{G_{opt}}{\omega_o C_{gs}} = \alpha\sqrt{\frac{\delta}{5\gamma}(1 - |C|^2)} \quad (10)$$

Consider the drain current expression for a short-channel transistor in saturation [2];

$$I_D = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)(V_{gs} - V_{th})\left[(V_{gs} - V_{th})\|(LE_{sat})\right] \quad (11)$$

And equation from [1] below;

$$Q_S = \frac{1}{\omega_o\left(\frac{2}{3}WLC_{OX}\right)R_S} \quad (12)$$

An optimum condition will occur when the quality factor of the source is at its optimum,

$$W_{opt} = \frac{3}{2\omega_o LC_{OX}Q_{S,opt}R_S} \quad (13)$$

Hence, the size of the transistor is shown to have a link with the noise factor.

From Noh, 2010 state that Q in the range of 3.5 and 4.5 will achieve an approximately constant power dissipation for the same value of noise figure [4]. So, in this paper, $Q_{opt}$ is taken to be 3.9 and the related parameter that been used is listed in the Table I below.

TABLE I. PARAMETER VALUE

| Parameter | Specification |
|---|---|
| ω□ | 2Π (2.14GHz) |
| L | 0.13µm |
| $C_{ox}$ | 15.145 mF/cm |
| $to_x$ | 2.28 x $10^{-9}$ m |
| $R_s$ | 50 Ω |
| $Q_{in\ opt,\ PD}$ | 3.9 |
| $\mu_n$ | 220$cm^2$/Vs |
| $L_g$ | 14.3nH |
| $C_d$ | 100fF |
| $R_1$ | 7 kΩ |

Since the $L_d$ is required to resonate with Cascode $C_d$ at 2.14 GHz, their relationship can be expressed by;

$$\omega_d = \frac{1}{L_d C_d} \tag{14}$$

*B. Voltage Biasing Circuit*

After the width of transistor $M_1$ is determined, the next step is to set the biasing voltage. Voltage supply to the LNA is 1.2V. The I-V characteristic of W µm transistor was plotted was varied from 0 to 1.2 V. If the $V_{DS}$ across $M_1$ and $M_2$ is taken as 0.6 V each (for mid-point biasing to maximize voltage swing at M1, it is found that for the $V_{GS}$ in the range of 0.3 V to 0.4 V, the corresponding current flowing through M1 is from 1mA to 3.9 mA. The $V_{GS}$ versus current obtained from this experiment is tabulated and given in Table II.

TABLE II. $V_{GS}$ AND $I_D$ FOR W µM TRANSISTOR

| **$V_{GS}$ (V)** | 0.33 | 0.35 | 0.37 | 0.38 | 0.39 | 0.40 |
|---|---|---|---|---|---|---|
| **$I_D$ (mA)** | 1.0 | 1.6 | 2.39 | 2.84 | 3.34 | 3.9 |

Table II shows the current consumed by the amplifying transistor only and a small allocation need to be reserved for the current consumed by the on chip biasing circuitry. Another plot is carried to obtained $g_m$ for a variation of $V_{GS}$. $V_{TH}$ can be determined by using below equation;

$$V_{TH} = V_{GS} - \frac{(g_m L)}{\mu_n C_{ox} W} \tag{15}$$

TABLE III. $V_{GS}$ AND CORRESPONDING $V_{TH}$ W µM TRANSISTOR

| **$V_{GS}$ (V)** | 0.36 | 0.37 | 0.38 | 0.39 |
|---|---|---|---|---|
| **$g_m$ (A/V)** | 0.04884 | 0.05486 | 0.06106 | 0.06739 |
| **$V_{TH}$** | 0.2943 | 0.2960 | 0.2978 | 0.2990 |

It is show that the value of $V_{TH}$ is 0.29 V. In order to give an overdrive voltage of 100 mV, $V_{GS}$ need to be 0.39 V.

Since $M_3$ is a biasing transistor, its W/L ratio should not be big in order to prevent large current consumption. $M_3$ forms a current mirror with $M_1$.

## IV. RESULT AND DISCUSSION

Circuit in **Figure 1** was simulated using Cadence SpectreRF. Models parameter was provided by Silterra (Malaysia). Figure 2, illustrate the performance of forward and reverse gain of the simulated LNA. It is shown that the propose LNA achieve to get $S_{21}$ of 18.24 dB at 2.14 GHz, while $S_{12}$ is -42.17dB.

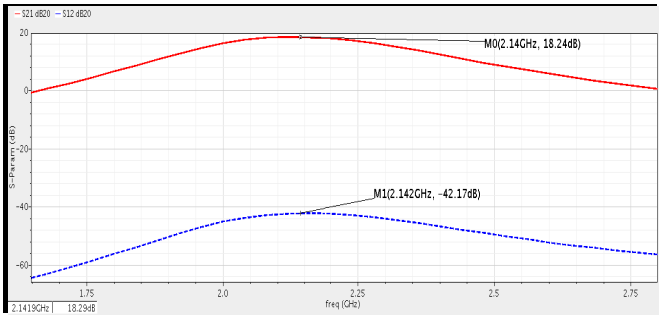


Figure 2. Forward Gain ($S_{21}$) and Reverse Gain ($S_{12}$)

Figure 3 shows the input and output coefficient of the LNA. Peak $S_{11}$ value at 2.14GHz is 19.5dB while $S_{22}$ value is-13dB. This is shown that the LNA has good input and output matching.

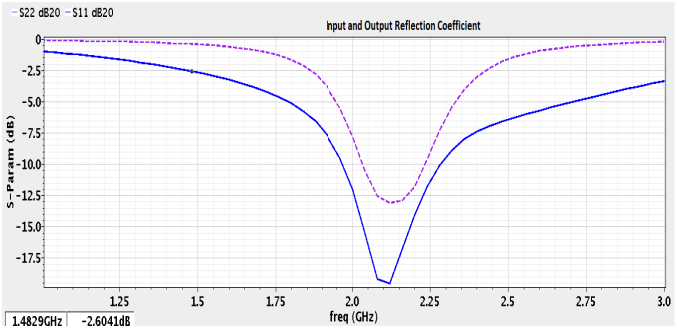


Figure 3. Input Reflection Coefficient ($S_{11}$) and Output Reflection Coefficient ($S_{22}$)

Besides forward gain,$S_{21}$, Noise figure, NF is the most important parameter in designing the LNA. In this inductively degenerated LNA, the noise figure achieves to get as low as 1.362 dB as shown in Figure 4 below.

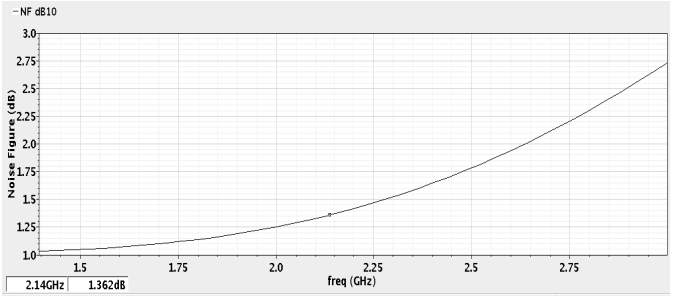


Figure 4. Noise Figure

The simulated results are shown in Figures 2 to 5. The resulted 1.326 dB noise figure from the simulation shows that an inductively cascode degeneration

amplifier can function well as a low noise amplifier. In terms of gain, the LNA gain, $S_{21}$ of 18 dB is within the requirement.

In terms of linearity fulfilment, the circuit is able to pass the test as input-referred IIP3 is 2 dBm (above the required –l dBm) and input 1-dB compression point is -13 dBm. Figure 5 show the IIP3 and input 1-dB compression point.

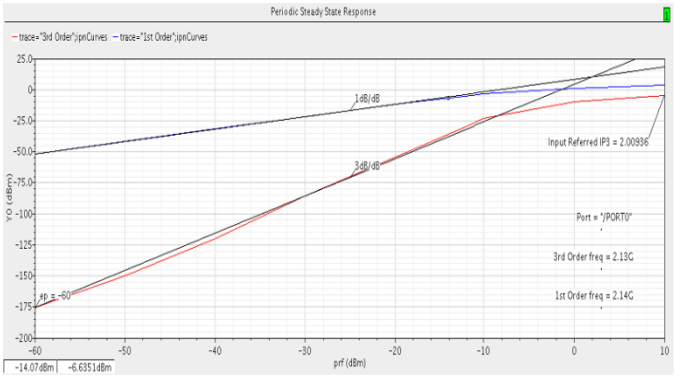


Figure 5. IIP3

Table III shows a summary of the performance of the LNA obtained from simulation. The targeted values are based on the W-CDMA specification.

TABLE III. RESULTS SUMMARY

| Specification | Targeted | Simulation |
|---|---|---|
| NF(dB) | <2 | 1.362 |
| S11, input reflection coefficient (dB) | <-10 | -19 |
| S12, reverse isolation (dB) | <-10 | -42.17 |
| S21, forward power gain (dB) | >15 | 18.24 |
| S22, output reflection coefficient (dB) | <-10 | -13 |

The simulation result presented in this work is comparable to other research publish by others. The chosen published performances are mixed of architecture and technology. Table IV summarizes the performance of the propose design along with other published results. From the table, it can be concluded that the inductively source-degenerated cascode present a better performance although the circuit is supply by a low power. It can be seen that the LNA design based on the proposed methodology demonstrates a competitive gain and the lowest noise figure among others.

TABLE IV. COMPARISON LNA PERFORMANCE AND OTHER PUBLISHED WORKS

| Author [Ref], Year | This work 2011 | Z.M.Lin [5] 2007 | N.M.Noh [6], 2006 | K.C.Wan [7] 2005 |
|---|---|---|---|---|
| Architecture | PCNO + Inductively degenerated cascode | Current reuse | Differential + inductively degenerated | Dual band + Source degenerated cascode |
| Frequency, GHz | 2.14 | 2.14 | 2.14 | 2.4 |
| Supply voltage, V | 1.2 | 1.0 | 1.8 | 1.8 |
| Technology (µm) | 0.13 | 0.18 | 0.18 | 0.18 |
| NF(dB) | 1.362 | 3.5 | 1.4 | 2.9 |
| S11 (dB) | -19 | -12 | -11 | -10.1 |
| S21, (dB) | 18.24 | 20 | 11 | 10.1 |

## V. CONCLUSION

This paper had focused on circuit design techniques that would allow the implementation of analog circuits at low power supply voltages in a standard CMOS technology. In this work, a low-voltage of 1.2V, 0.13µm RFCMOS utilizing inductively degenerated cascade LNA topology is proposed. The design methodologies employ power constraint noise optimization to achieve low noise and good input and output matching. The simulation results validate peak performance at 2.14 GHz which make the LNA suitable for WCDMA application. A low noise figure of 1.326 dB and power gain of 18.24 dB is achieved at the resonance frequency.

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