Analog and Short Channel Effects Performance of Sub-100 nm Graded Channel Fully Depleted Silicon On Insulator (SOI)

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Abstract – This paper presents the dependency of analog and Short Channel Effects (SCEs) performance of 75 nm channel length fully-depleted Silicon On Insulator (SOI) device on the applied Graded Channel (GC) design. The comparative analysis between standard SOI (STD SOI) devices at doped channel and equivalent threshold voltage, V_{TH} with GC SOI device are examined on the basis of internal physical mechanisms. Device characterizations are performed using simulation based approached provided by ATLAS 2D. Results show superiority of GC performances over standard SOI devices in both analog and SCEs point of views.

Keywords :- Graded Channel Fully Depleted SOI, SOI, analog, Short Channel Effects (SCEs)

1 Introduction

By the year of 2020, CMOS process technology for RF and analog applications is expected to be further down scaled to as low as 11nm, mainly to achieve the requirement to produce high performance device with even lower power supply [1]. The classical SOI structure is therefore forcing to be renewed, incorporative with several semiconductor engineering elements in order to meet such expectations. One of the emerging device concepts being discussed is the Graded Channel (GC) structure. Several papers have been published revolving on this channel design alternative, adopted onto many kind of silicon based structures such as MOSFET, SOI MOSFET and GaAs devices. Furthermore, sufficient analysis coverage on different aspects of device performances including analog and radio frequency (RF), high and low frequency noise and distortion properties as well as practical circuit applications have been demonstrated in the analytical, simulated or fabricated methodology for long channel device with physical gate length dimension beyond 1 μm [2-8]. These initial efforts are then extended for channel length down to 0.1 μm [9]. The objective of this work is to develop a fully depleted GC SOI device in the sub-100 nm dimension particularly using 75 nm channel length design, with comparative analysis on standard SOI structure. Results obtained are discussed in the physics based framework in which accounting on the influences of surface potential, electrical field and carrier velocity profiles.

2 Device Simulation Conditions

The schematic cross section of the GC SOI structure is as shown in Fig.1. Device characteristics are simulated using ATLAS 2D, activating on several models such as fldmob, conmob, cvt, srh, auger, etc to account on electrical field dependent, concentration dependent, inversion layer and minority carrier recombination respectively [10]. Model properties of both GC SOI and STD SOI are as summarized in Table 1 showing that both device types are sharing same structural properties with two different STD SOI models available. STD A is fully doped channel STD SOI with doping concentration equivalent to the highly doped region, N_{HD} of GC SOI, while STD B is fully doped channel STD SOI with modulated concentration having same value of threshold voltage, V_{TH} with GC SOI. This is to provide a fair performance assessment.

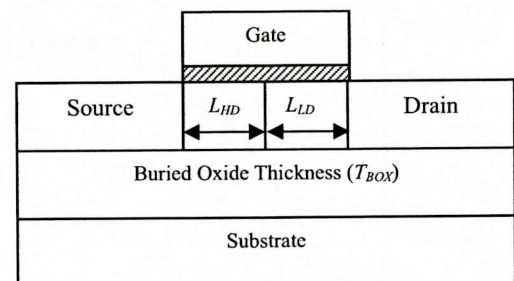

Fig.1 Schematic cross section of SOI model used

Based on fig.1, GC device is developed by masking the threshold voltage adjust ion implantation at drain side (L_{LD}), preserving the natural wafer p type doping in this region. Thus, the effective channel length, L_{EFF} of GC device which is reduced to the region within L_{HD} is

Table 1 Summary of investigated model properties

Properties \ Types	GC SOI (GC)	STD SOI A (STD A)	STD SOI B (STD B)
S/D Doping (cm^3)	5×10^{22}		
Silicon Thickness, T_{Si}	25 nm		
Buried Oxide Thickness, T_{BOX}	75 nm		
Gate	n+ poly		
Channel Length	$L_{HD} + L_{LD}$ =75 nm		
Channel Doping (cm^3)	3×10^{18}	3×10^{18}	2.309×10^{18}
Channel Properties	$L_{HD} : L_{LD}$=1:1	$L_{HD} : L_{LD}$=1:0	$L_{HD} : L_{LD}$=1:0

the first important approximation made for further results analysis and discussion.

The main output to be focused were subthreshold, *S* parameter, on-state current, I_{ON}, transconductance, g_m, and output conductance, g_D which further determine the device achieveable intrinsic gain, A_V, and both linear and saturation threshold voltage, V_{TH_lin} and V_{TH_sat} in which used for Drain Induced Barrier Lowering (DIBL) measurement. V_{TH_lin} and *S*-parameter are extacted from gate characteristic plot under fixed drain bias, V_{DS} = 0.05 V. Transconductance, g_m and V_{TH_sat} were also obtained from gate characteristics but at V_{DS} = 1.0 V. The output characteristics on the other hand yield the on-state current, I_{ON}, and output conductance, g_D values.

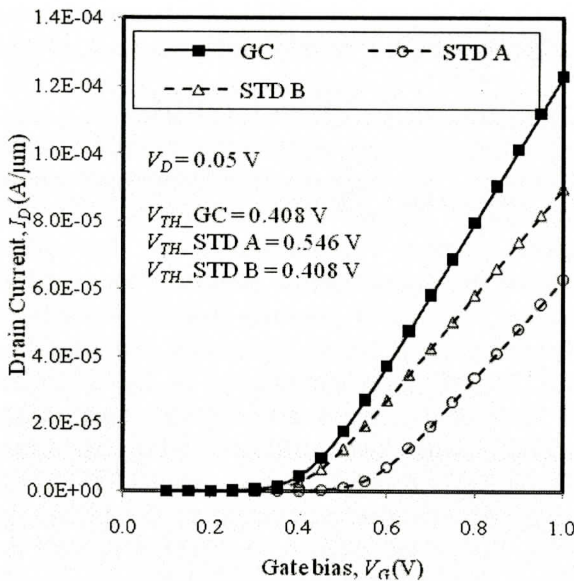

Fig.2 Gate characteristic

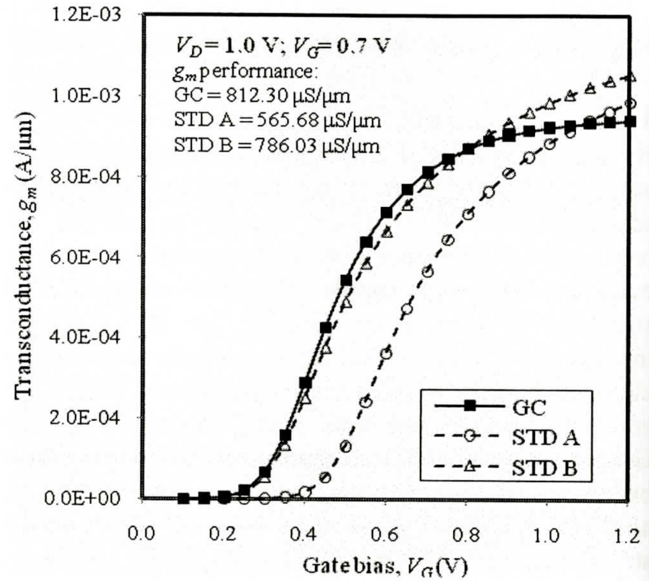

Fig.4 Transconductance characteristic

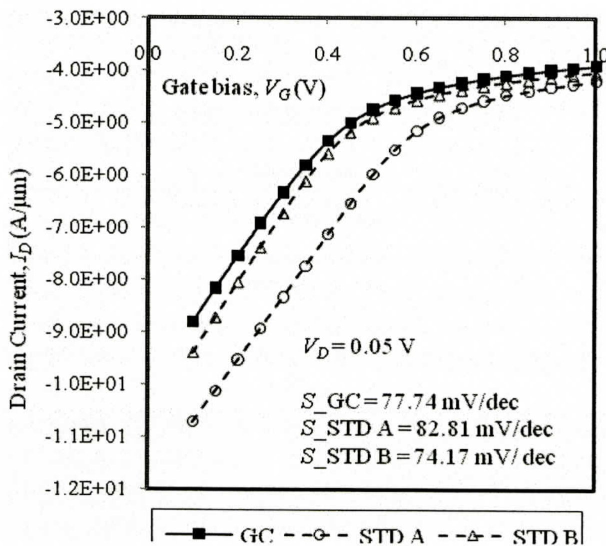

Fig.3 Subthreshold characteristic

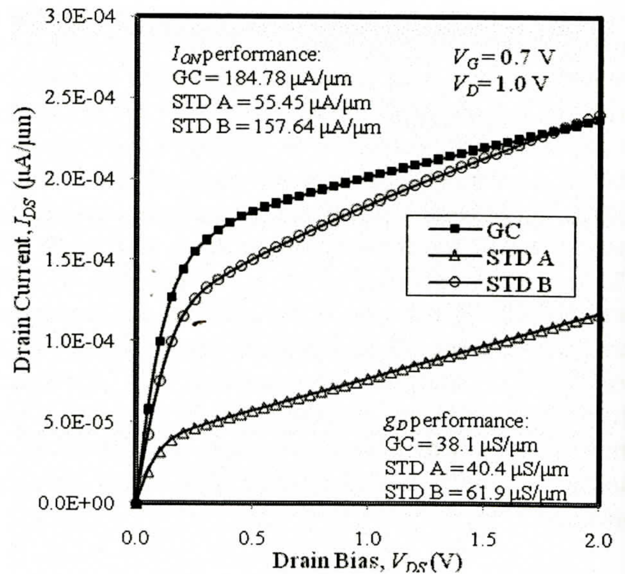

Fig.5 Output characteristics

3 Results and Discussion

Fig. 2 and 3 show the resultant curves of gate characteristics in subthreshold regime when $V_{DS} = 0.05$ V. It is apparent from fig. 2, that the applied GC has the advantage of improved carrier transport efficiency as compare to standard SOIs, with either same channel doping level or same threshold voltage setting [11]. Taking the inverse logarithmic of the obtained gate characteristics, the subthreshold, S parameters are determined using the following mathematical expression [12].

$$S = \left(\frac{\partial \log I_D}{\partial V_G}\right)^{-1} = \left(\frac{\partial \ln I_D}{\partial V_G}\right) \quad mv/dec \qquad (1)$$

Table 2 Overall performance results

Types / Performance	GC SOI (GC)	STD SOI A (STD A)	STD SOI B (STD B)
V_{TH_lin}	0.407 V	0.546 V	0.407 V
	0.256 V	0.319 V	0.230 V
	152 mV/V	227 mv/V	178 mv/V
	77.7 mV/dec	82.8 mV/dec	74.2 mV/dec
	184.8 μA/μm	55.5 μA/μm	157.6 μA/μm
	812.3 μS/μm	565.7 μS/μm	786.0 μS/μm
	38.1 μS/μm	40.4 μS/μm	61.9 μS/μm
	21.3	14.0	12.6

green : excellent, yellow : satisfactory, red : worst

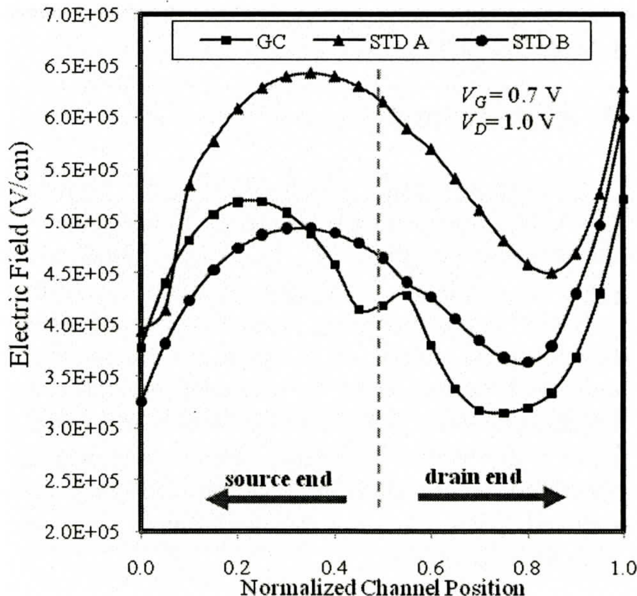

Fig.7 Electric field profiles comparison

In the subthreshold regime, GC design is showing a satisfactory result, whereby the GC S-factor measurement is slightly higher than the standard SOI model with same V_{TH} value but is much better compared to STD A model. Next the transconductance, g_m trends are plotted in fig.4 which are obtained by taking the first derivative of the gate characteristics at fixed $V_{DS} = 1.0$ V as given in below equation [12].

$$g_m = \frac{\partial I_D}{\partial V_D} \quad S/um \qquad (2)$$

Based on this figure, the advantage of higher g_m by adopting GC structure for these particular structural properties can only be achieved at gate bias, V_G below

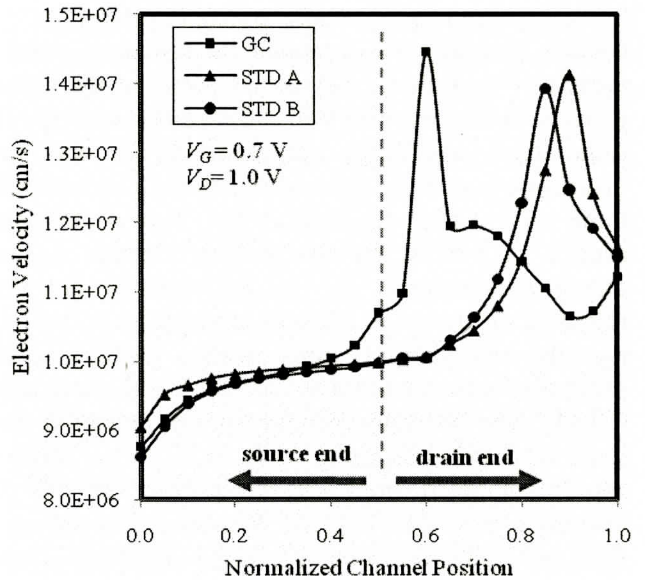

Fig.6 Electron velocity profiles comparison

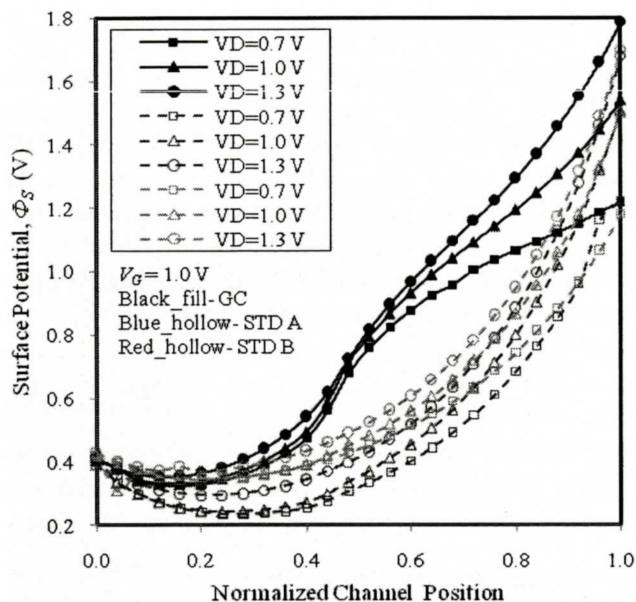

Fig.8 Surface potential profiles comparison

0.8 V. Therefore the operating or reference point is taken at V_G = 0.7 V, whereby GC SOI has the highest g_m performance over the two standard SOI models. The same bias conditions are applied for the next evaluation in order to observe the output characteristics trend of models developed. The two performance aspects of interest are the on-state current, I_{ON} and output conductance, g_D. g_D performance not only reflected on device achievable intrinsic gain, but also describe the short channel effects (SCEs) in the saturation regime known as channel length modulation (CLM). The on state current, I_{ON} are extracted from these output characteristics at $V_D = V_G - V_{TH}$, while g_D can be obtained from the slope taken beyond the saturation point [11-12],[18]. Results are as shown in fig.5 whereby GC device exhibit excellent output characteristics performance with highest I_{ON} and lowest g_D compare to both standard SOI models developed in this work. The overall performance results are as summarized in table 2. Included in this table are the intrinsic gain and DIBL results where again GC shows superior advantage over the conventional SOI structure. Furthermore, the performance enhancement was observed in all analog figure of merits selected in this work for GC design except for satisfactory in subthreshold parameter point of view.

In order to explain the theoretical insights that are responsible for the enhanced performance observed in GC structure, the surface potential, electrical field and electron velocity profiles are probed along the channel. Better I_{ON} and g_m performances demonstrated in GC design are the outcome of the enhanced carrier transport efficiency in which can be visualized by the higher carrier velocity overshoot, that is located nearer to the channel portion near the source end as given in fig.6 [13-16]. By comparing GC and STD B in fig.7, GC model provides higher electrical field peak near the source region thus promoting the accelerated force of charge carriers resulted in enhanced carrier injection into the channel. Although the field peak near the source end in GC is the second highest, it is distributed along smaller portion of effective channel length, L_{EFF} [13-16]. This phenomenon causes highest velocity overshoot at the L_{HD} and L_{LD} interface thus improved carrier transport is obtained. Whereas for STD A and STD B, highest field peak in STD A causes slightly higher overshoot in the electron velocity profile compare to STD B, but higher doping density used in STD A itself has the effect to degrade carrier mobility hence the peak moves nearer to drain side [17]. Therefore, lowest I_{ON} and g_m are obtained in STD A as stated in table 2.

Improvement in g_D and DIBL with the applied GC are the consequences of surface potential behaviour along the channel as well as electrical field profile observed at the channel portion near the drain side. Electrical field profile at drain side of GC device in fig.7 is lower than both STD A and B hence resulted on improved Hot Carrier Effect (HCE) and DIBL as given in table 2 [11][18]. Fig.8 on the other hand, shows the surface potential profiles comparison in the saturation regime whereby the obtained plots explained on the better output conductance as shown in Fig.5. The improved performance is therefore attributed to the fact that practically all V_{DS} increased dropped across the channel portion with lower doping concentration. In other words, L_{HD} becomes the effective channel length whereby this portion is screened from higher drain potential variation while channel region with lower concentration act as drain extension [18-19]

4 Conclusion

Simulation studies which describe the performance of GC SOI was critically discussed in this paper. From the obtained results, GC SOI was found to be a potential candidate for enhanced analog performance, in order to push scaling limit beyond the predicted technological trend. GC structure remain to show enhanced performance in terms of on-state current, transconductance, output conductance and open loop gain with better reliability issue management in threshold, subthreshold and saturation regime through reduced DIBL, *S*-parameter and output conductance with the applied GC.

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