Design and Implementation of Single-Phase Hybrid Active Power Filter Controller

N. A. Rahim
Dept. of Electrical Engineering
University of Malaya
50603 Kuala Lumpur, Malaysia
email: nasrudin@um.edu.my

S. Mekhilef
Dept. of Electrical Engineering
University of Malaya
50603 Kuala Lumpur, Malaysia
email: saad@um.edu.my

I. Zahrul
Dept. of Electrical Engineering
University of Malaya
50603 Kuala Lumpur, Malaysia
email: zahrul@hotmail.com

Abstract-This paper presents a combination of a series active power filter and a shunt passive filter. The shunt passive filter is connected in parallel with a load and suppresses the harmonic current produced by the load, whereas the active filter connected in series to a source acts as a harmonic isolator between the source and load. For active filter control, Sinusoidal Pulse Width Modulation (SPWM) is developed and the modulation index is selected by calculating the DC bus voltage of the active filter. The PSpice®, Matlab/Simulink® and MAX PLUS II® softwares are used for simulation and hardware implementation.

Keywords: Active filter, harmonic compensation, power quality

I. INTRODUCTION

Harmonic distortion can be classified as voltage harmonic and current harmonic. The effects of voltage harmonic distortions are voltage sag, swell and fluctuation. The main causes of this distortion are sudden loading of the system at the common coupling point, large neutral currents due to unbalance loading, improper grounding and etc [1]. These effects result the voltage drops in supply line impedances, generation of earth-neutral voltage and interference in communication system. Process control system can often lead to data loss and malfunctioning of protective relay. The primary effects of current waveform distortions are power factor reduction, poor utilization of distribution wiring plant, high current flow in the neutral line of four-wire three-phase system and the dangerous over heating of cable and etc [1-2]. These current harmonic results an increases in the level of rms supply current, power loss, heating of equipment, increase the reactive power demand. [3].

Harmonic problem can be minimized by the following three ways:

i) By adding passive or active harmonic filters to attenuate the harmonic problems.

ii) The utilization of auto-transformer to the phase shift section of the load in such a manner as to cancel low order harmonics.

iii) By replacing the existing power distribution transformers with the transformer that include phase shifted winding on the secondary and/or that have high level of reactance between the primary and secondary windings. The next breakthrough in active filter development has resulted from the starting of microelectronic revolution.

Starting from the use of discrete analog and digital components, the progression is going to microprocessors, micro-controllers and Digital Signal Processors (DSPs). It is possible to implement complex algorithm on-line for the control of active filter at reasonable cost. This development has made it possible to use different control algorithms such as, Proportional Integral (PI), variable–structure control, fuzzy logic and neural nets for improving the dynamic and steady state performance of the active filter. With this improvement, the active filters are capable of providing fast corrective action even with dynamically changing non-linear loads [3-4].

Active filter basically, is a voltage or current source PWM inverter. It has been studied and put into practical use because they have the ability to overcome the disadvantages inherent in passive filters. The active filter of voltage or current source inverter has variable current or voltage source. It eliminates the harmonics by injecting the compensating current or voltage direct to the AC lines. The complete cancellation of harmonics will be achieved if the filter generates the compensating current equal and opposite to the present harmonics or compensating voltage in phase with the system. In practice, the ideal compensating would be achieved by the different modulation method [4-6].

Harmonic elimination by active power filter is entirely dependent upon the modulation method. The most useful methods of modulation are carrier wave modulation and pulse width modulation. In carrier wave modulation method, carrier wave modulation suppresses the harmonic content to the small amount by adjusting the magnitude and the frequency of carrier wave. In order to reduce the harmonics, it is necessary to raise the carrier frequency, but it causes the more complex control circuit, and it increases the switching loss. The PWM such as the multi pulse scheme can solve the harmonic compensation problems, and multi pulse PWM active filter has good characteristics of harmonic elimination. However, this filter needs the compensating source of constant current or voltage [3-6].

A new Active Filter has been proposed in this paper on the basis of the combination of Active Power Filter and passive elements such as capacitor and reactor to eliminate the voltage and current harmonic of the load. As a result the proposed system can solve the problems inherent in using only the passive filter. In addition active filter is much smaller in rating than a conventional active power filter.

II. PROPOSED TOPOLOGY

The single line diagram of the Active Power Filter is shown in Figure 1. A single-phase voltage source inverter is connected in series between the ac source and a single-phase full bridge diode rectifier with a non-linear harmonics producing load. This configuration is known as Active Power Filter. A passive filter is connected in parallel before the load at the load end.
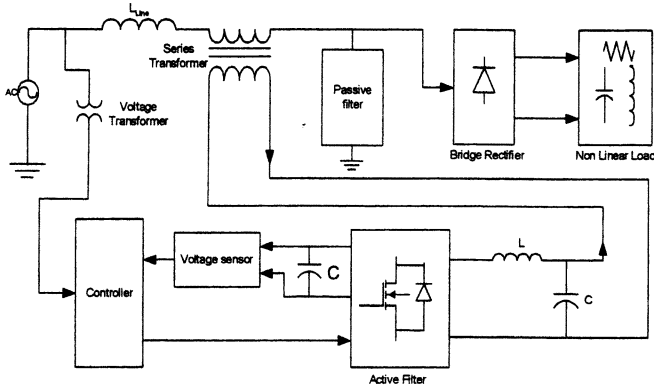

Fig. 1. System configuration of hybrid active power filter

In this configuration passive filter bypasses the current harmonic component according to the designed value of the passive element and the Active Filter acts as a voltage compensator and harmonic isolator between the source and load. The voltage compensation is done by injecting the in-phase voltage to the line. The harmonic isolation is also done by this series compensation, which behaves as active impedance, which does not cause any voltage drop for the fundamental component, but it forces to pass the current harmonic component through the passive filter. Thus the Active Filter improves the filtering characteristics of passive filter and the power factor of the load by compensating the reactive power required by the load.

In active technology there is no additional DC voltage source for the inverter. A diode bridge is connected parallel to the inverter and a large capacitor is connected to the DC side of the rectifier or inverter. The capacitor acts as a DC source for the inverter and it stores the energy on OFF switching state of inverter-bridge.

For inverter control harmonic current detection is a well-known technique. Instantaneous reactive power theory, Fast Fourier transforms method (FFT), Analog notch filter (low pass, high pass and band pass filter) and active and reactive power calculation method is widely used for this purpose. In this project a new control approach is implemented.

Figure 2 shows the block diagram for the control of an Active Power Filter. A sinusoidal reference waveform is compared with a triangular carrier waveform to generate gate signals for the switches of the inverter. The amplitude of the modulating wave (reference waveform) is obtained by multiplying a fixed amplitude sine wave with the amplitude of a variable processed signal, which is the key parameter for the inverter out put voltage control in shape and amplitude. This

processed signal is extracted by comparing DC bus capacitor voltage with a reference DC value. The error signal (difference between the DC bus voltage and the DC reference voltage) is processed by a Proportional, Integral and Derivative (PID) controller for stability.
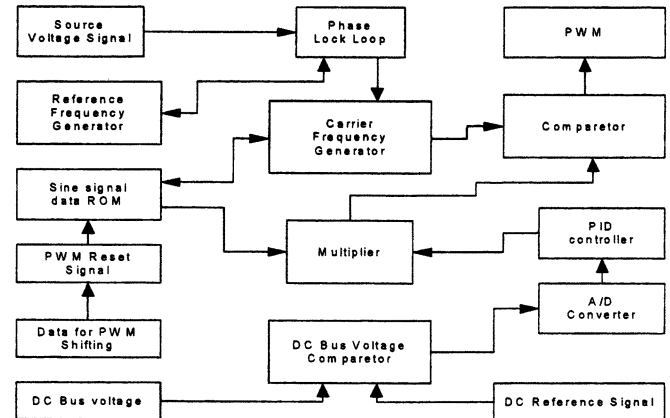

Fig. 2. Block diagram for the control of an active power filter.

III. SYSTEM IMPLEMENTATION

Practical implementation of an Active Filter control was digitally implemented on an Altera Field Programmable Gate Array (FPGA). FPGA is an integrated circuit (IC), which consists of an array of logic elements either gates, look up tables, RAM, flip-flop and programmable interconnected wiring that can be programmed in the field after manufacture by a technique. Altera development tool converts the design idea into configurable data file, which could be loaded into Altera FPGA.

For the implementation of sinusoidal PWM a regular sampling technique is used. A carrier wave is compared with the modulating wave (amplitude*sine wave). The real time generation of a sine wave using Altera is time consuming. An alternative approach is that to store the sine values in the look up table, which is programmed in permanent memory (PROM). A sine voltage equation is used to generate data for sinusoidal waveform. An up-down counter is used to read the data from ROM. Each counting value determines the address of ROM for each data.

Triangular carrier is also generated by an 8-bit UP-Down counter and some peripheral logic gates. The counter is clocked externally by a clock generated from the phase lock loop. The rate at which the UP-Down counter incremented or decremented is determined by main clock frequency. When the counter starts counting in up direction and goes to maximum, some logic gates monitor it and generates a signal for down counting. Similarly when the counter reaches to minimum counting value, the monitoring logics interrupts the counting and the counter changes it counting direction and the process repeats continuously. One UP-Down counting completes one cycle for triangular carrier.

Figure 3 shows the top level schematic for PWM generation, every step of carrier wave is compared with

modulating wave, which is obtained by digital multiplication of sine value from ROM and a control signal (amplitude) from the closed loop control. The comparison between the carrier and modulating signal had to be done in a manner that when the carrier value is less than or equal to the modulating signal the PWM output level is high and when the carrier value is greater than the modulating value the PWM output level is low. The comparison is done in every clock pulses that means in every step of counting for carrier values as well as for the ROM data value. This comparison time fully depends on the design of PWM circuit and the main clock frequency.
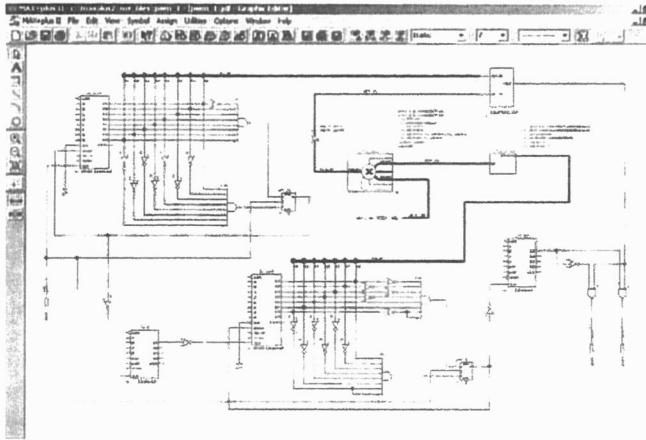
Fig.3. PWM scheme using max plus II®

The main clock frequency is generated by a Phase Lock loop (PLL). This main clock frequency, 9.83MHz is adjusted precisely for the carrier frequency 19.2KHz.

In closed loop control the amplitude of the modulating wave is determined by comparing the DC bus voltage with a DC reference voltage. The difference of this two DC values is converted to digital value and processed by a PID controller for stability.

The digital realization of PID controller is implemented by bit serial algorithm. In PID control proportional represents the gain of a signal. The digital division and multiplication is used to represent the gain. Integration disappears the steady state error of a signal. To obtain the integration of a present value, it is added with the previous integrated value. The derivative of a signal is widely used in controller to achieve good dynamics. In digital realization, differentiator is the gradient between two samples. To implement the difference equation, a sample has to be passed in pipeline for one sampling period and then be subtracted from the current sample. Adder values can under flow or over flow, so it must be controlled properly.

IV. SIMULATION RESULTS

The simulation results are obtained by simulating the model shown in Figure 1 by MATLAB/ SIMULINK. The plot shown in Figure 4 (a) represents the simulated source voltage

and the source current with out compensation by Active and passive filter. Figure 4 (b) represents the harmonic spectrum of the source current shown in Figure4 (a), which was analysed by MATHCAD software and the total harmonic distortion is 32.6%.
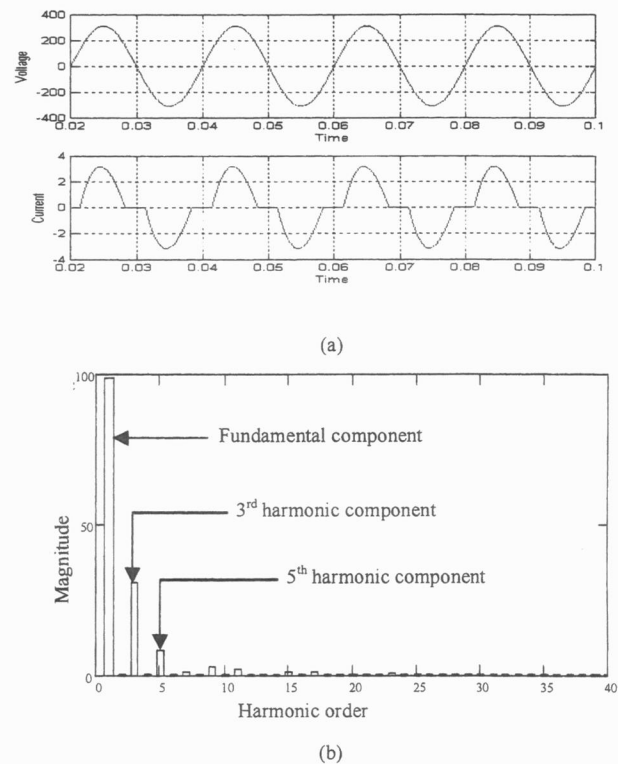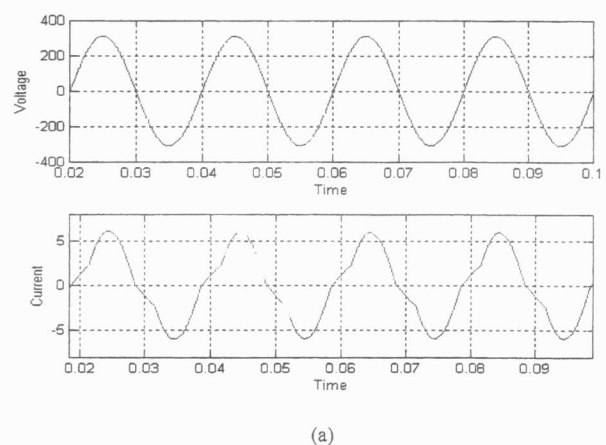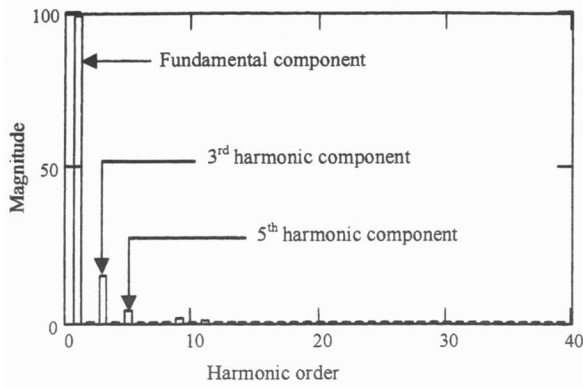

(a)

(b)

Fig. 4: a) Simulated source voltage and current without compensation by active and passive Filter (b) Harmonic spectrum of source current

Figure 5(a) and Figure 5 (b) illustrates the simulation results for the source voltage and the current, and the harmonic spectrum of the source current with the compensation by the passive filter only. The total harmonic distortion is 16%.
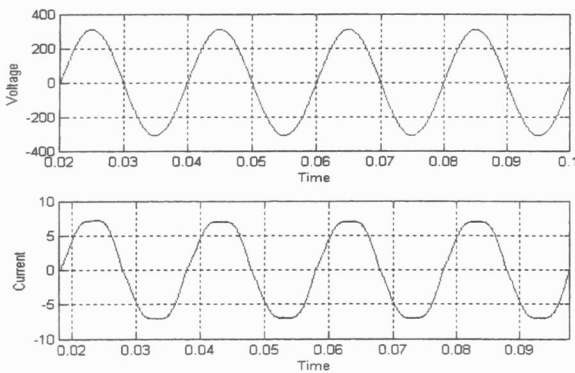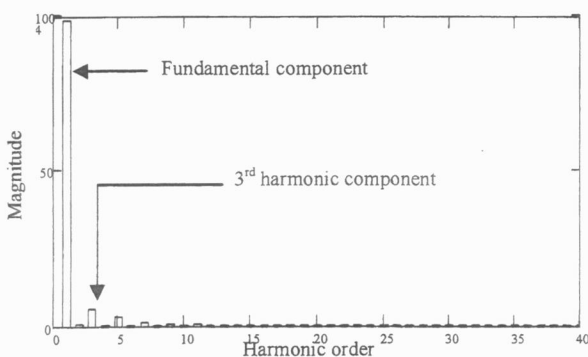

(a)

(b)

Fig. 5 (a) Simulated source voltage and current after compensation by only passive filter (b) Harmonic spectrum of source current

Figure 6 (a) and Figure 6 (b) show the simulated source voltage and current, and the harmonic spectrum of source current after compensation by active and passive filter and the total harmonic distortion is 6.7%.

Figure 7 shows the simulated voltage and current source wave pattern in same axis, which represents that the voltage and current source are almost in-phase.

(a)

(b)

Fig.6 (a) Simulated source voltage and current after compensation by active and passive filter (b) Harmonic spectrum of source current
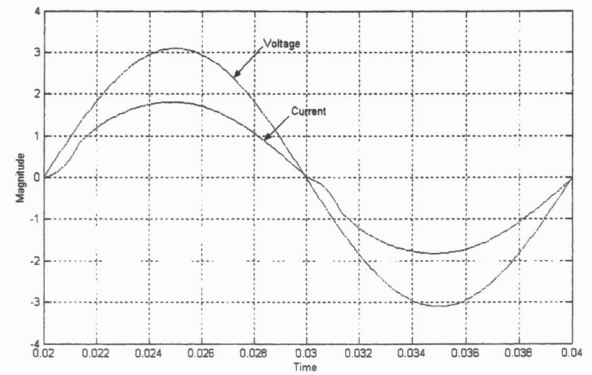

Fig. 7. In-phase pattern of simulated voltage and current source
(Scale: For voltage 100V/div., for current 2A/div.)

XY plot represent the phase displacement and the rough distortion idea about the two waves, if there is phase displacement between the two waves, the XY plot become elliptical in shape and without phase displacement between the waves, the XY plot become as a straight line with minimum distortion. For harmonic distorted wave the XY plot has no standard shape. From the XY plot it is also possible to measure the phase displacement of two waves.
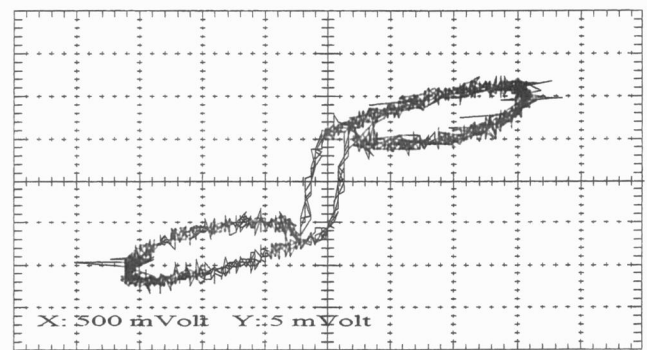

Fig.8. XY plot of voltage and current source before compensation

Figure 8 shows the XY plot of voltage and current source without compensation and with compensation by active power filter and passive filter.

V. CONCLUSION

Many configurations of active power filters are available to compensate the harmonic current, reactive power, neutral current, and also the unbalance current of the harmonic load. The proposed active power filter can compensate current harmonics components, reactive power and also improves the power factor of the load. The results show the active filter reduces the total harmonic distortion up-to 7.78%. Without active and passive filter, 3rd harmonic and 5th harmonic distortion was 37.98% and 6.47% respectably. After compensation by active and passive filter both reduces to 5% and 2.13%.

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