

## Direct Torque Control Permanent Magnet Synchronous Motor Drive with Asymmetrical Multilevel Inverter Supply

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**Abstract**—This paper demonstrates the Direct Torque Control Permanent Magnet Synchronous Motor (DTC-PMSM) drive fed by asymmetrical multilevel inverter. The cascaded H-bridges topology with ratio-3 dc voltage sourced cells inverter has been employed. The DTC controller receives a reference torque and flux signals, the torque controller output determines the position of the desired flux vector. The amplitude of this vector is determined by the reference flux amplitude. The reference voltage vector is calculated as a continuous value using a technique developed originally for the SVM controlled drive. In this study, however, the reference voltage vector has been approximated to the nearest voltage vector achievable by one switching state of the multilevel inverter. The performance of two- and three-cells per arm inverter drives has been compared to that of the SVM-inverter drive at two values of the switching intervals. The results reflect the low switching frequency and torque ripple advantages of the proposed scheme.

### I. INTRODUCTION

The direct torque control (DTC) concept has been originally developed for induction motor drives and it has been well accepted by manufacturers and attracted researchers' attention [1]. It is known that the high torque ripple problem associated with the basic DTC scheme can be eased by effectively increasing the inverter's output resolution. Many developments have been introduced to achieve this such as zero state modulation [2], space vector modulation (SVM) [3] and the use multilevel inverter [4]. In general these modified schemes provide the desired torque smoothing and the price is added switching losses or power circuit complexity.

The DTC technique has been extended to the permanent magnet synchronous motor (PMSM) drives [5, 6]. The advantages of the DTC-PMSM drive compared to other PMSM drives are eliminating the current control and axis transformation besides the capability to operate without position sensor [7]. The torque ripple problem associated with the hysteresis comparators and switching table controller has been treated by introducing the PI controller and the SVM inverter [8, 9]. The SVM-DTC drive combines the basic DTC advantages with the torque and flux ripples reduction provided by the SVM technique, but it requires more powerful processor and operate at higher switching frequency.

The application of modified converter circuits has been considered recently in the PMSM-DTC drives to obtain improved characteristics. The three-level inverter has been used with four-level flux and torque hysteresis controllers and consequently modified switching table [10]. The comparison with the basic two-level system has shown the

harmonic and switching frequency reduction advantages. Another study replaced the rectifier-inverter supply by a matrix converter [11]. The matrix converter based DTC-PMSM drive has been operated in two modes; Basic DTC scheme and SVM-DTC. It has been shown that the matrix converter can maintain unity power at the supply side.

Among the multilevel inverter topologies, the cascaded H-bridge inverter has the advantages of modular structure and simple design. This topology is well suited for asymmetrical multilevel inverter implementation achieved by supplying the cascaded cells by different values of dc voltages and results increased number of levels for a given inverter circuit [12]. The maximum number of levels can be achieved by an inverter with "*c*" H-bridge cells per arm is  $3^c$  and this occurs when the dc supplies voltages of the cascaded cells are related by ratio 3, i.e.  $V_s, 3V_s, 9V_s, \dots$  etc. [13]

In this paper, ratio –three sourced asymmetrical multilevel inverter is considered for the PMSM-DTC drive. Due to the large number of voltage vectors obtainable, it is not practical to consider the extension of the switching table based-DTC. Therefore the control concept is extracted from the SVM-DTC drive presented in [8] and [9]. This paper compares the performance of two- and three-cells inverter to that of the SVM-inverter fed drives. Up to our knowledge, this is the first report of the application of the ratio-three based multilevel inverter in a DTC drive.

Section II describes the asymmetrical multilevel inverter. Section III presents the continuous voltage reference DTC strategy and the related equations. In section IV the Multilevel inverter PMSM-DTC model is presented. Simulation results are presented in section V.

### II. RATIO-THREE BASED SOURCED CASCADED H-BRIDGES MULTILEVEL INVERTER

#### A. Circuit Topology, Switching States and Voltage Vectors

A three-cell per arm cascaded H-bridge inverter is shown in Fig. 1a. As seen the three cells of each arm are fed by dc voltages of  $V_s, 3V_s$  and  $9V_s$  respectively. Each cell can be controlled to produce zero, the positive, or negative of its input. Therefore the arm voltage has a maximum of  $13V_s$ , i.e. the sum of the three dc voltages, and a minimum of  $-13V_s$  and 27 levels as seen in Fig 1b.

The inverter seen in Fig 1 is three-cell or 27-steps inverter it can produce 2107 voltage vectors, where the *c*-cells per arm inverter has  $3^c$  levels and the *l*-level three-phase inverter has *v* of distinct voltage vectors given in (1).

$$v = (l)^3 - (l - 1)^3 \quad (1)$$

The switching state of the inverter to be represented by three numbers  $[x_a, x_b, x_c]$ , where  $x_a, x_b$  and  $x_c$  represents the switching state of arms a,b and c respectively. For  $c$ -cells per arm inverter:  $x_{a,b,c}$  take any integer within the range

$$-\frac{3^c-1}{2} \leq x_{a,b,c} \leq +\frac{3^c-1}{2} \quad (2)$$

With respect to the common point of the three inverter arms, N in Fig. 1a, the line voltage can be represented by:

$$\begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = V_s \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (3)$$

The load line-to-line voltages and the balanced load phase voltages expressions are given in (4) and (5) respectively

$$\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = V_s \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} = \frac{V_s}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (5)$$

Where  $n$  is the load neutral point, not shown in the figures. The output voltage vector corresponding to an inverter state is give by:

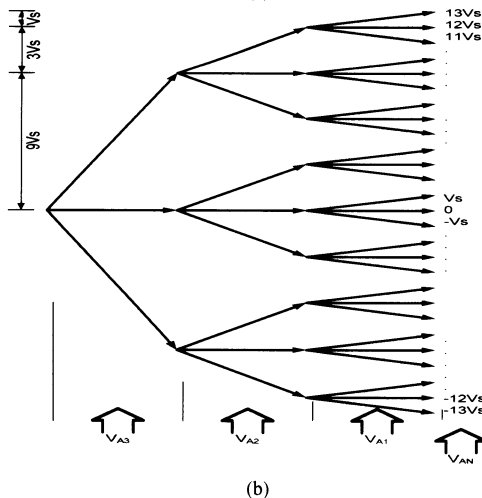
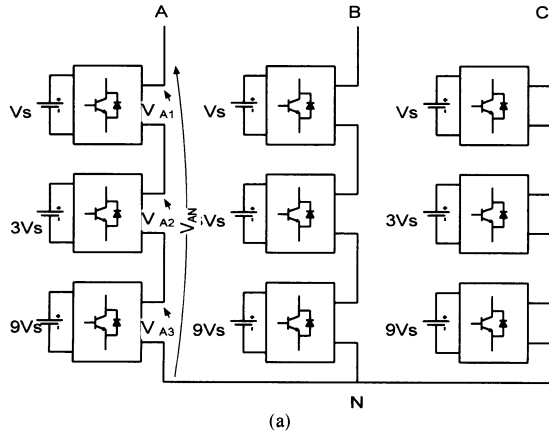


Fig. 1. (a) 3-cell, 27-level asymmetrical cascaded H-bridge inverter (b) the voltage levels corresponding to one inverter arm.

$$\vec{v}_o = v_d + jv_q = \left[ \left( x_a - \frac{x_b}{2} - \frac{x_c}{2} \right) + j \left( \frac{\sqrt{3}x_b}{2} - \frac{\sqrt{3}x_c}{2} \right) \right] V_s \quad (6)$$

### B. Voltage Vector Control

While the advantage of the based-3 ratio sourcing is to maximize the number of levels for a given number of cascaded cells, PWM-control is not suitable with this condition. The reason is that certain state transitions between adjacent voltage levels involve the high voltage cell switching results in high switching frequency of these cells [14]. Therefore, voltage vector control of this inverter has been redefined as operating the inverter in the state that produces the voltage vector nearest to the reference vector rather than constructing the reference vector by adjusting the duty ratio of three inverter vectors.

The best one state vector approximation of a given reference voltage vector ( $\vec{v}_o^* = v_d^* + jv_q^*$ ) can be realized by first analysing the reference vector to its reference phase voltage components:

$$\begin{bmatrix} v_d^* \\ v_b^* \\ v_c^* \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & 0 \\ -1 & \sqrt{3} \\ -1 & -\sqrt{3} \end{bmatrix} \begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} \quad (7)$$

Then approximating the normalized phase reference voltages to the nearest integers, results the inverter switching state:

$$x_{a,b,c} = \text{round} \left( \frac{v_{a,b,c}^*}{V_s} \right) \quad (8)$$

where *round* represents the rounding towards the nearest integer. The phase switching state ( $x_{a,b,c}$ ) is converted to the corresponding phase cascaded cells desired gains ( $X_{c1}$ ,  $X_{c2}$  and  $X_{c3}$ ) using a look up table as shown in Fig. 2 for the three-cell inverter.

## III. DTC-PMSM DRIVE WITH CONTINUOUS REFERENCE VOLTAGE

### A. The motor equations

The stator side equations of the PMSM motor in the rotor reference frame are:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} R_s + pL_d & -\omega L_q \\ \omega L_d & R_s + pL_q \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 \\ \omega \varphi_f \end{bmatrix} \quad (9)$$

where  $v_{d,q}$  and  $i_{d,q}$  are the motor voltage and current components, related to the actual quantities by the inverse transformation of equation (7),  $R_s$ ,  $L_d$  and  $L_q$  are the stator circuit resistance and direct and quadrature inductances,  $\omega$  is the electrical synchronous speed and  $\varphi_f$  is the rotor flux. And the motor torque expression is given by

$$T_M = \frac{3p_p \varphi_s}{4L_d L_q} [2\varphi_f L_q \sin \delta + \varphi_s (L_d - L_q) \sin 2\delta] \quad (10)$$

where  $p_p$  is the number of pole pairs and  $\delta$  is the angle between the stator and rotor flux vectors referred to as the torque angle. The motor torque is proportional to  $\sin \delta$  and can be controlled by changing this angle

#### B. Reference voltage calculation

The DTC controller used has PI torque controller its output signal  $\Delta\delta^*$  represents the desirable change in the torque angle over the next switching signal. The new reference stator flux has an angle equals to the current angle of the stator flux plus  $\Delta\delta^*$ . The flux amplitude is taken as a constant this amplitude must abide to the stability condition derived in [5] and given by:

$$\varphi_s < \frac{L_q}{L_q - L_d} \varphi_f \quad (11)$$

The controller determine the stator flux that is required to be build up during the next switching state as shown in Fig. 3, where

$$\Delta\varphi_s^* = \varphi_s^* - \varphi_s \quad (12)$$

Where  $\varphi_s$ ,  $\varphi_s^*$  and  $\Delta\varphi_s^*$  are the estimated, next reference, and desired change of the stator flux respectively.

The stationary dq-model stator side voltage equation is given by

$$\vec{v}_s = \vec{i}_s R_s + p\varphi_s \quad (13)$$

Therefore the next reference stator voltage vector is defined as:

$$\vec{v}_s^*(k) = \vec{i}_s(k-1)R_s + \frac{\Delta\varphi_s^*}{T_s} \quad (14)$$

where  $T_s$  is the switching interval. This voltage vector is realized using the method described in section II.B

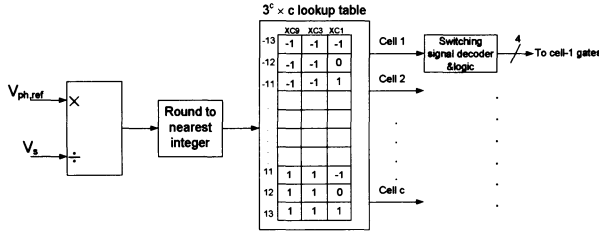


Fig. 2. Multilevel inverter control by the following phase reference voltage (the table shown inside the lookup table block for 3-cell per arm inverter)

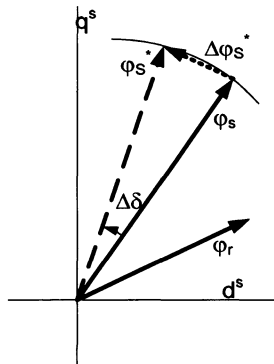


Fig. 3. Stator reference flux and flux difference calculation

#### IV. DRIVE MODEL DESCRIPTION

The drive controller is constructed based on (9) - (14) and the multilevel inverter as shown in Fig. 4. The parameters of the PMSM are given in Table I. The DTC converter is operated at a sampling time of 100 and 50μsec and the PI torque controller gain is set to  $K_p=1250$  and  $K_i=0.9 \times 10^6$ , the output of the controller is multiplied by a constant equivalent to the switching time, not shown in Fig. 4. The summation of the dc voltages for one inverter arm is 195V. The load is modeled by a pure friction torque of 0.033441 N.m.sec. For comparison, a different model has been constructed for the SVM DTC drive with the same motor and controller parameters and SVM controller with voltage control time step equals to 1% of the torque loop time interval,  $T_s$ .

In the following section, the reference torque has been set to a constant value of 3.6 N.m. and the reference stator flux amplitude is set to a constant of 0.7Wb. The results compare the performance of the three flowing system:

- 1) SVM –inverter controlled DTC-PMSM drive
- 2) 2-cell per arm asymmetrical cascaded H-bridge inverter fed DTC-PMSM drive
- 3) 3-cell per arm asymmetrical cascaded H-bridge inverter fed DTC-PMSM drive

#### V. SIMULATION RESULTS AND DISCUSSION

With the model parameters described in section IV, the DTC -PMSM drive has been simulated from starting over 0.4 sec. During the switching interval,  $T_s$ , the multilevel inverter holds the state corresponding to the voltage vector nearest to the reference voltage vector. On the other hand, the SVM drive produces the reference voltage vector by adjusting the duty ratios of two nonzero adjacent inverter states and the zero states during this interval.

##### A. Torque ripple

The simulation results are plotted in Fig. 5 and Fig. 6 for switching intervals of 100 and 50μsec respectively. It can be seen from Fig. 5 that the 3-cell multilevel inverter drive has a peak-to-peak torque ripple of about 20% of that of the SVM drive. At this sampling time, the 2-cell per arm inverter, or the nine-level inverter has a torque ripple slightly less than that of the SVM inverter. At switching interval of 50μsec the SVM drive inverter ripple decreases considerably, however, the torque ripple of the multilevel inverter drives is almost not affected as seen in Fig. 6.

The unaffected torque level with the time interval variation is due to the fact that this limit is set by the inverter resolution. By comparing the torque levels at the two switching intervals, it seems that we can define an optimum sampling time as the longest sampling time beyond which the torque ripple reduction is negligible.

It has to be indicated here that the SVM voltage controller operates at switching time equals to 1% of  $T_s$ . This implies that the SVM drive requires much faster processor and faster switching devices than the proposed multilevel scheme. However, the proposed multilevel inverter operation cannot be further improved by PWM technique, due to the fact that the high voltage cells will be subjected to high frequency operation which eliminates the hybrid structure advantage.

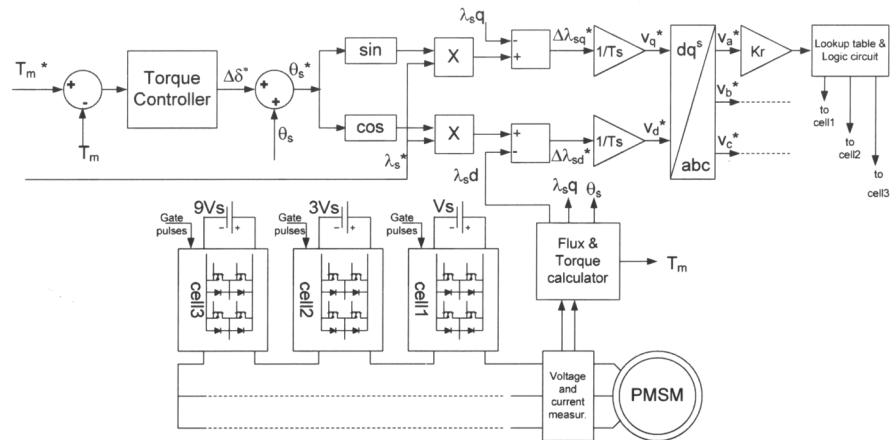


Fig. 4 The proposed multilevel inverter DTC-PMSM drive system

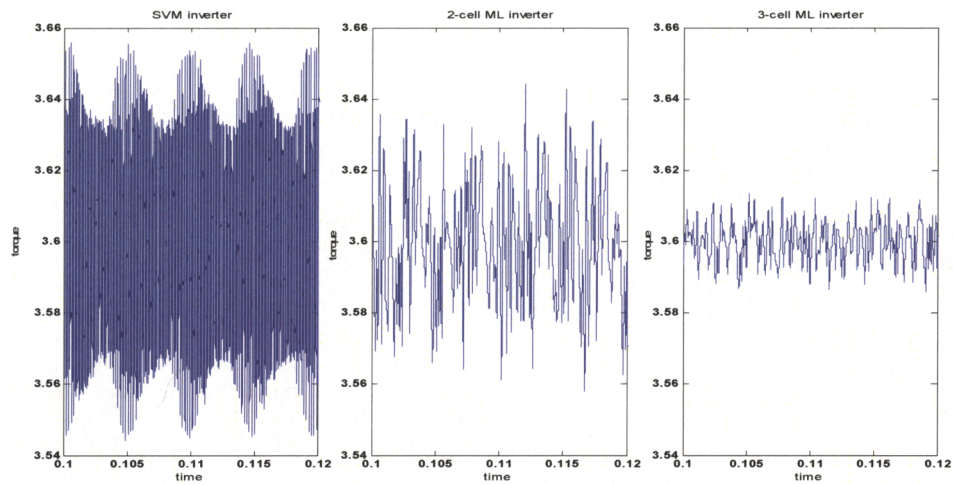


Fig. 5. The torque ripple comparison of the DTC-PMSM drive with, from left, SVM controlled inverter, 2-cell per arm and 3-cell per arm asymmetrical multilevel inverters with switching interval of 100μsec.

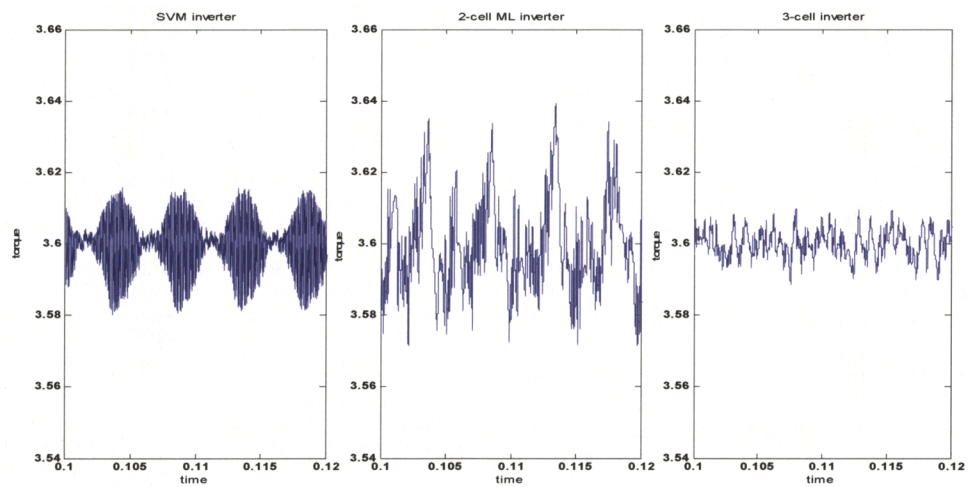


Fig. 6. The torque ripple comparison of the DTC-PMSM drive with, from left, SVM controlled inverter, 2-cell per arm and 3-cell per arm asymmetrical multilevel inverters with switching interval of 50μsec.

TABLE I  
PARAMETERS OF THE IPMSM USED IN THE COMPUTER  
SIMULATION

Rated output power (W)	1000
Rated phase voltage (V)	138.56
Magnetic flux linkage (Wb)	0.533
Number of poles	4
Rated torque (N.m)	6
Maximum speed (rpm)	1500
Stator resistance ( $\Omega$ )	5.8
d-axis inductance (mH)	44.8
q-axis inductance (mH)	102.7
Moment of inertia of the motor and load ( $\text{Kg}\cdot\text{m}^2$ )	0.001

### B. Switching losses

As an indication of the switching losses, the sum of switching pulses for the three switching signals has been plotted over the simulation period. Also the multilevel inverter pulses has been counted for the individual H-bridge legs. The results are given in Fig 7 and Fig. 8 for 100 $\mu\text{sec}$  and 50 $\mu\text{sec}$  switching intervals respectively. It can be seen that the SVM inverter switch operates at an average switching frequency close to 5kHz when the sampling time is 100 $\mu\text{sec}$  and to 10kHz with sampling time of 50 $\mu\text{sec}$ . This rate consists with the basic SVM concept where the switching period is twice the sampling time. The multilevel inverter switching frequency for the lowest voltage switch is only about a quarter of this value and for the higher voltage cell is less by few orders. The total number of switching pulses obtained by adding the pulses for the cascaded cells is also shown. The total number of switching pulses forms about one third of the number of the SVM inverter for the three-cell inverter and about one quarter for the 2-cell inverter. This implies a considerable saving in the switching losses.

Another related advantage of the multilevel inverter that should be mentioned is related to the switching pattern. Whereas, the switching frequency (1/100 or 1/50 $\mu\text{sec}$ ) represents the maximum switching frequency for the multilevel inverter switching devices, it forms twice the averages frequency for the SVM inverter. The difference is that the average switching frequency gives indication about the switching losses, but the maximum switching frequency is required to determine the switching device speed. If the SVM criteria of 100 steps per switching interval is followed, it implies that the switching device is subject to operate at a switching speed of 2 $\mu\text{sec}$  or 1 $\mu\text{sec}$  for the two tested switching intervals. In other words the required switching frequency rating of the fastest (low voltage's cell) multilevel inverter switching device is 50 times less than that of the SVM controlled inverter.

## VI. CONCLUSION

The cascaded H-bridge cells asymmetrical multilevel inverter has been proposed to supply the PMSM-DTC drive. Two and three cells per arm inverters have been considered.

The DTC control strategy is similar to the one used for the SVM DTC-PMSM drive. This strategy produces a continuous reference voltage vector. The inverter controller approximates this reference vector to the nearest vector that can be produced by one inverter switching state, and the inverter holds this state during the following switching interval.

The proposed drive system has been modeled and, for the purpose of performance evaluation, it has been compared with the SVM drive of the same switching interval. The results obtained demonstrate that the 2-cell drive has a torque ripple level comparable to that of the SVM drive, and the 3-cell drive has a torque ripple level much lower than the SVM drive at switching interval of 100 $\mu\text{sec}$ . However, the results show that the SVM torque ripple reduces by decreasing the switching time interval while the torque ripple of the multilevel inverter, with the proposed controller, has a minimum ripple level after which increasing the controller frequency does not reduce it. By comparing the number of switching pulses per arm it has been shown that the multilevel drive has much lower switching losses compared to the SVM drive.

Besides the advantages of the torque ripple and the switching losses reduction, the proposed drive inherits the features of the asymmetrical multilevel inverter drive, such as low voltage stress and the highest power stage operates at the lowest switching frequency.

The drive has two main drawbacks; first the higher number of switching devices and second the requirement for a number of dc power supplies equal to the number of H-bridge cells applied. However it sensible to suggest the system for battery powered drives or for high power or high voltage drives

Other aspects may be further investigated, issues like: modifying the inverter topology to accommodate SVM technique to reduce the ripple and developing a dedicated DTC concepts for this type of inverters.

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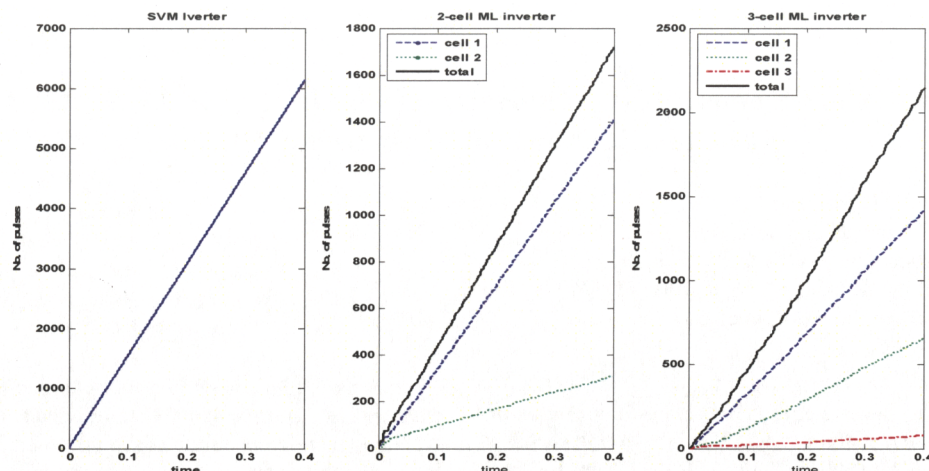


Fig. 7. The number of switching pulses of the three switching signals of DTC-PMSM drive with, from left, SVM controlled inverter, 2-cell per arm and 3-cell per arm asymmetrical multilevel inverters with switching interval of 100 $\mu$ sec.

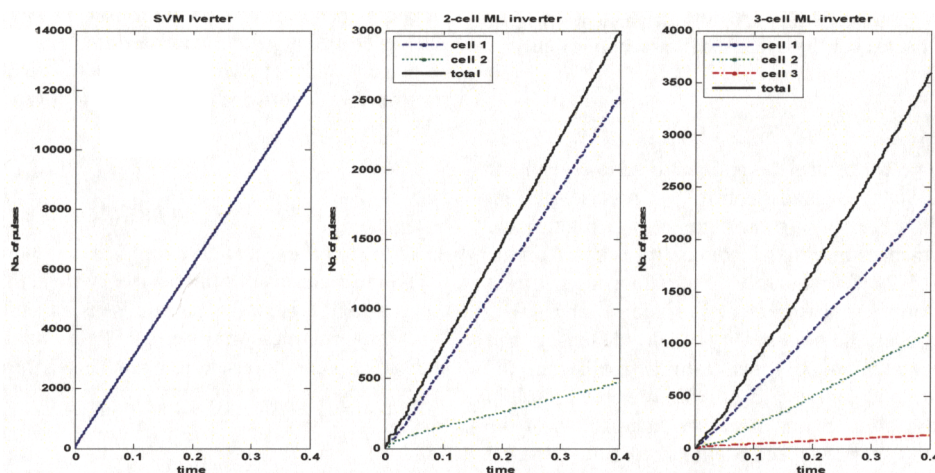


Fig. 8. The number of switching pulses of the three switching signals of the DTC-PMSM drive with, from left, SVM controlled inverter, 2-cell per arm and 3-cell per arm asymmetrical multilevel inverters with switching interval of 50 $\mu$ sec.

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