A Three-Phase Three-Level Voltage Source Inverter with a Three-Phase Two-Level Inverter as a Main Circuit

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Abstract

This paper proposes and describes the design of a three-phase three-level nine switch voltage source inverter. The proposed topology consists of three bi-directional switches inserted between the source and the full-bridge power switches of the classical three-phase inverter. As a result, a three-level output voltage waveform and significant suppression of the load harmonics contents are obtained at the inverter output. The harmonics contents of the proposed multilevel inverter can be reduced by half compared with the two-level inverter. A Fourier analysis of the output waveform is performed and the design is optimized to obtain the minimum total harmonic distortion. The full-bridge power switches of the classical three-phase inverter operate at the line frequency of 50Hz, while the auxiliary circuit switches operate at twice the line frequency. To validate the proposed topology, simulation and analysis have been performed. In addition, a prototype has been designed, implemented and tested. Selected simulation and experimental results have been provided.

1 Introduction

The output voltage of the conventional two-level inverter is so far from a sinusoid. The output voltage waveform total harmonic distortion (THD) ratio is approximately 31% [1]. In addition, in case of high power, it makes the use of the conventional inverters very rare due to the power switches have to withstand the full network voltage.

There are some proposed solutions in [2] – [6], where these topologies are formed from two cells of the classical two-level inverter topology. The outputs of these cells can be added together using injection transformers [2] - [4] or directly by connecting the output of one cell in series with another [5] – [6]. As a result, the harmonic content of the output voltage is significantly reduced.

Multilevel inverters (MLIs) can be used to solve these problems. They are built using a number of cells; each cell consists of switches and capacitor voltage sources. The control of the power switches allows the capacitor voltage sources to be added to obtain the desired output voltage at reduced voltage stress on each individual switch. Besides, the resolution of the staircase waveform of the output voltage increases with the number of voltage steps of capacitor voltage sources available in the multilevel inverter. Three different main topologies have been reported for multilevel inverters: 1) diode-clamped or neutral-clamped [7]–[8], where the dc-bus voltage is split into (n+1) levels by n capacitors, where the middle point is called the neutral point; a number of diodes clamp the stress voltage on the power switches; 2) capacitor-clamped or flying capacitors [9]–[10], where additional capacitors are used to clamp the switches voltage stress; 3) cascaded multi-cell with separate dc sources [3], [11], and [12], where each phase leg consists of n similar cells connected in series, each cell formed from a switched capacitor and four power switches. All these solutions are relatively simple for getting a three-level staircase waveform, but become extremely complicated for getting a higher multilevel staircase waveform.

2 The Proposed Inverter Topology

The block diagram of the proposed three-phase three-level voltage source inverter system consists from two isolated and regulated dc sources, three-level inverter, microcontrollers, data acquisition card PCL-818L, and a personal computer as shown in figure 1. This system acts as a link between the output of the linear generator and the load, where the linear generator output voltage magnitude is single phase distorted waveform with frequency varying from 25 to 50 Hz. Thus it is not suitable for many applications, which use 50 Hz ac. The inverter output voltage can be controlled by controlling the dc inverter bus link voltages, where two dc-dc boost converter circuits with 10 kHz switching frequency have been used. The measured voltages of the inverter dc capacitor link (two analogue signals) from the sensors are received first by microcontroller1 and microcontroller2 which convert them to 8 bits digital signals for each analogue signal (16 bits total). These 16 digital bits are received by the PC through the PCL-818L card.

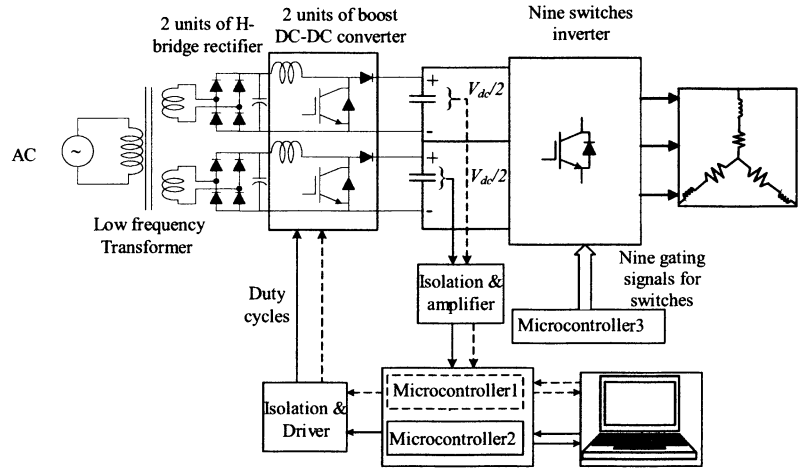

Figure 1: Block diagram of the proposed inverter and the feedback control circuit.

The digital data is processed in real time to calculate the duty cycle of each dc-dc converter using PID controller. The sampling frequency is chosen to be 2 kHz which is fast enough to perform these calculations. These duty cycles subsequently are sent back to the hardware through the PCL-818L card in a digital form. Microcontroller1 and Microcontroller2 receive these digital data from the PCL-818L card and converts them to a duty cycle required by each switch in the dc-dc converter. Microcontroller3 is used to generate the inverter nine controlling pulses. In order to avoid short circuit during transition between switches of each leg, a proper time delay has been considered.

Figure 2 shows the proposed inverter, which consists of two isolated H-bridge circuit units; and capacitor banks C_1 and C_2, respectively; conventional two-level inverter Q_1 through Q_6 as a main inverter at 50 Hz switching frequency; and an additional circuit which compromises of bi-directional (middle) switches S_1 through S_3, at 100 Hz switching frequency, which allows energy to flow in both directions.

3 Analysis of the Optimized Waveform

The operation can be divided to 12 switching states. The switch on/off states is shown in Table 1. By applying the switching patterns given in figure 3, the node 'a' referred to point '0V' can be defined as follows:

- For voltage level $v_{an} = V_{dc}$, turn on the upper switch Q_1.
- For voltage level $v_{an} = V_{dc}/2$, turn on the middle switch S_2.
- For voltage level $v_{an} = 0$, turn on the lower switch Q_2.

The switches conduction angles can be calculated from figure 4 as follows:-

for upper switches Q_1, Q_3, and Q_5

$$\theta_1 = \frac{4\pi}{3} - 2(\alpha_1 + \alpha_2) \quad (1)$$

for lower switches Q_2, Q_4, and Q_6

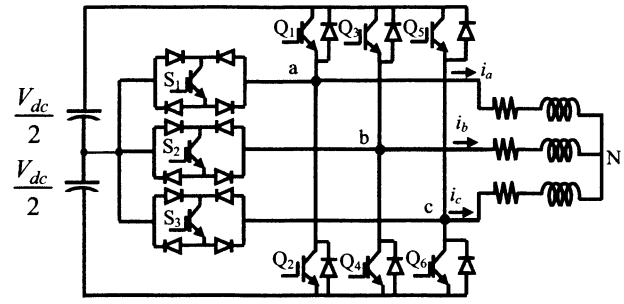

Figure 2: The proposed nine switches three-level inverter

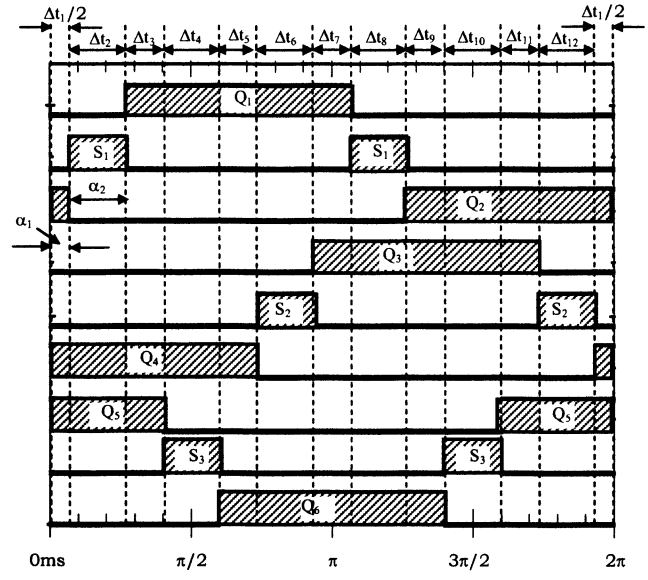

Figure 3: Switching timing diagram.

Step Duration	Conduction period	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	S_1	S_2	S_3
Δt_1	$2\alpha_1$	0	1	0	1	1	0	0	0	0
Δt_2	α_2	0	0	0	1	1	0	1	0	0
Δt_3	$2\alpha_1$	1	0	0	1	1	0	0	0	0
Δt_4	α_2	1	0	0	1	0	0	0	0	1
Δt_5	$2\alpha_1$	1	0	0	1	0	1	0	0	0
Δt_6	α_2	1	0	0	0	0	1	0	1	0
Δt_7	$2\alpha_1$	1	0	1	0	0	1	0	0	0
Δt_8	α_2	0	0	1	0	0	1	1	0	0
Δt_9	$2\alpha_1$	0	1	1	0	0	1	0	0	0
Δt_{10}	α_2	0	1	1	0	0	0	0	0	1
Δt_{11}	$2\alpha_1$	0	1	1	0	1	0	0	0	0
Δt_{12}	α_2	0	1	0	0	1	0	0	1	0

Table 1: Switching states of switches in each step duration.

$$\theta_2 = \frac{2\pi}{3} + 2\alpha_1 \quad (2)$$

for bi-directional switches S_1, S_2, and S_3

$$\theta_3 = 2\alpha_2 \quad (3)$$

Therefore from equations (1), (2), and (3), $\theta_1 + \theta_2 + \theta_3 = 360^\circ$

From figure 5 which illustrates the load phase voltages v_{an}, v_{bn}, and v_{cn} referred to the neutral of the dc bus. If the neutral point '0V' of the dc bus is not connected to the neutral point of the load 'N', the phase voltages of the load are related to the neutral point of the dc bus 'n' as given in [13] by the following equation.

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \quad (4)$$

The line-to-line load voltage v_{ab} can be obtained using the following equation:

$$v_{ab} = v_{an} - v_{bn} \quad (5)$$

From equations (4) and (5), the phase voltage of node 'a' v_{aN} and the line-to-line voltage v_{ab} can be calculated and drawn as shown in figure 5, the load phase voltage has 7 steps $(\frac{-2V_{dc}}{3}, \frac{-V_{dc}}{2}, \frac{-V_{dc}}{3}, 0, \frac{V_{dc}}{3}, \frac{V_{dc}}{2}$, and $\frac{2V_{dc}}{3})$ and the line-to-line voltage has 5 steps $(-V_{dc}, \frac{-V_{dc}}{2}, 0, \frac{V_{dc}}{2}$, and $V_{dc})$. The line-to-line voltage waveform as shown in figure 5 (b) is known as a stepped waveform. A Fourier analysis of this waveform gives the magnitudes of the harmonics as a function of α_1 and α_2 as in equation (6).

$$V_n = \frac{4(V_{dc}/2)}{n\pi}\{\cos(n\alpha_1) + \cos(n(\alpha_1 + \alpha_2))\},$$

$$n=1,3,5,..... \quad (6)$$

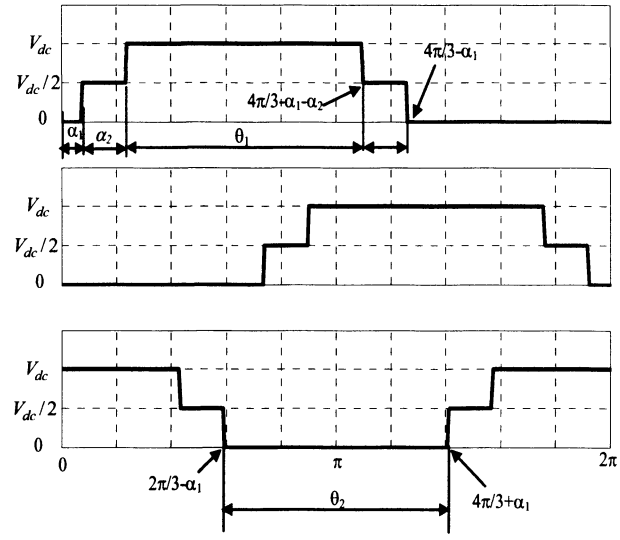

Figure 4: MATLAB SIMULINK simulated waveforms of the load node voltages v_{an}, v_{bn}, and v_{cn}

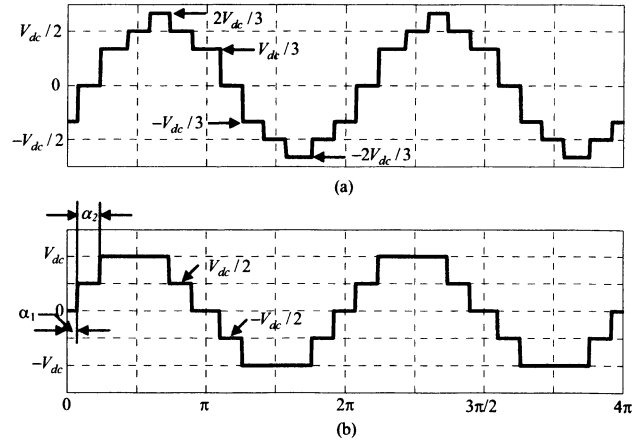

Figure 5: MATLAB SIMULINK simulated waveforms of:

(a) the load phase voltage waveform v_{aN}

(b) the line-to-line voltage waveform v_{ab}

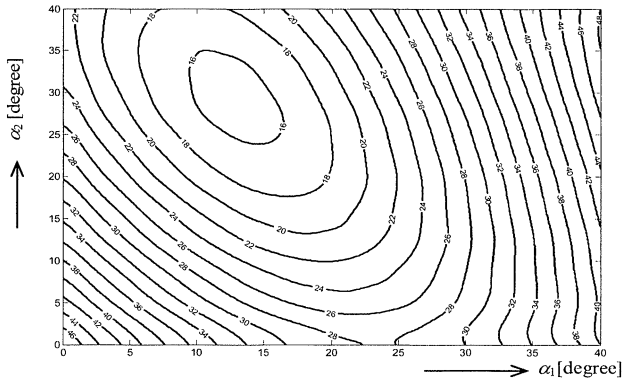

Figure 6. THD of the output voltage as a function of α_1 and α_2.

The ideal is to get a clean sinusoidal output voltage, i.e., the content of the harmonics orders greater than one (n=3, 5, 7 ...) should be zero. The THD of the output voltage defined as $\text{THD} = \frac{1}{V_1}\sqrt{\sum_{3,5,7,\ldots}^{\infty} V_n^2}$, where V_n is calculated from (6). The THD is shown in figure 6 as a function of the parameters α_1 and α_2. The computer simulation shows that the minimum THD (THD < 16%) is obtained for $\alpha_1 \approx 12^\circ$ and $\alpha_2 = 30^\circ$.

By comparing the proposed inverter which consists of 9 power switches and 12 main power diodes with the three-level NPC inverter which consists of 12 main power switches and 6 main power diodes [14] under fundamental frequency modulation, it can be concluded that, they produce the same output voltage waveform performance.

4 Results and Discussion

The proposed topology has been simulated using MATLAB/SIMULINK® to verify the performance of the proposed configuration. The dynamic response due to a sudden change in the reference voltage is presented and a Proportional Integral and Derivative (PID) controller has been implemented in order to maintain balanced voltages of the dc bus capacitor. A balanced three-phase star connected RL load with 30Ω resistance, and 50mH inductor per phase was used.

Figure 7 shows the inverter dc bus voltages of the upper and the lower capacitor banks respectively with controller, where a step change in the reference voltage from 80V to 110V is shown. Because the voltage of each capacitor is regulated to 80 V or 110 V, the total dc-link voltage is maintained at 160 V and 220 respectively. Figure 8 shows the inverter output waveforms of the phase voltage v_{aN}, line-to-line voltage v_{ab}, and the line current i_a. Where the phase voltage exhibits seven levels ($\frac{-2V_{dc}}{3}, \frac{-V_{dc}}{2}, \frac{-V_{dc}}{3}, 0, \frac{V_{dc}}{3}, \frac{V_{dc}}{2}$, and $\frac{2V_{dc}}{3}$), and the line-to-line voltage shows five levels ($-V_{dc}, \frac{-V_{dc}}{2}, 0, \frac{V_{dc}}{2}$, and V_{dc}). It is clearly shown that v_{aN}, v_{ab}, and i_a follow the step change in the DC capacitor voltage at 100ms.

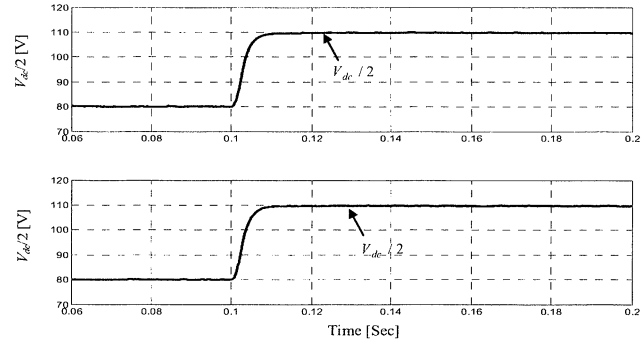

Figure 7: simulation results of the upper and lower regulated capacitor banks voltages.

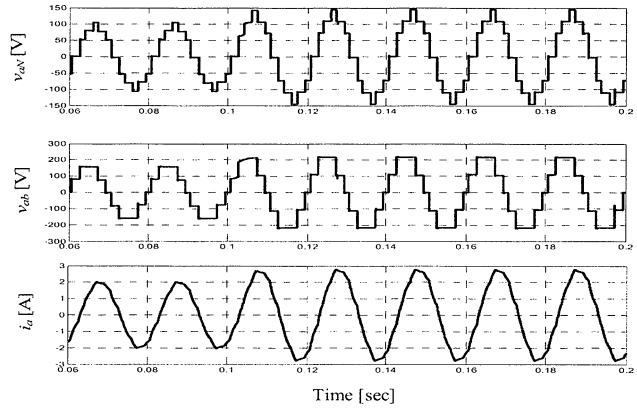

Figure 8: Inverter output (from top to bottom) phase voltage v_{aN}, line to line voltage v_{ab}, and line (phase) current i_a respectively.

To validate the proposed inverter, an experimental prototype of the proposed inverter has been built, experimentally tested, and compared with the simulation results. A balanced three-phase star connected load with 30Ω resistance, and 50mH inductor per phase was used. The inverter circuit was built using insulated gate bipolar transistors (IGBTs) as switches, and each bi-directional switch consists of one IGBT and 4 elements of fast diode rectifier. The inverter switching frequencies are 50 Hz for the conventional two-level inverter and 100 Hz for bi-directional switches. The control circuit switching frequency is 10 kHz which consists of 2 units of dc-dc boost converter.

Figure 9 shows a step change in the dc link capacitor voltage, where a step change has been applied from 80V to 110 V in each capacitor bank, thus maintaining 160V and 220V on the dc bus, respectively. Figure 10 shows the phase voltage v_{aN} with seven steps and the line-to-line voltage v_{ab} with five steps which have been verified in the simulation results. Figure 11 shows the phase voltage v_{aN} and the line current i_a.

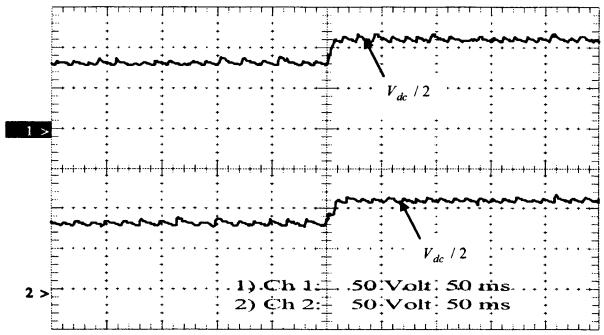

Figure 9: The inverter dc bus voltages (50V/div, 50ms/div).

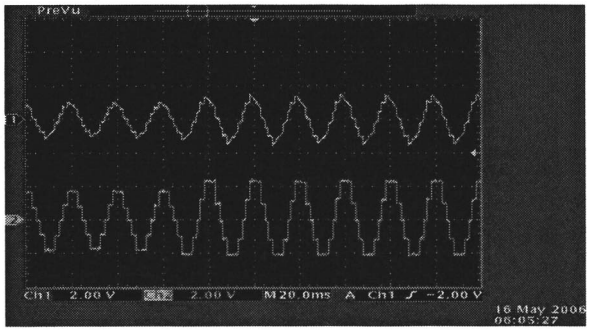

Figure 10: The load phase voltage v_{aN} and the line to line voltage v_{ab} (200V/ div, 20ms/ div).

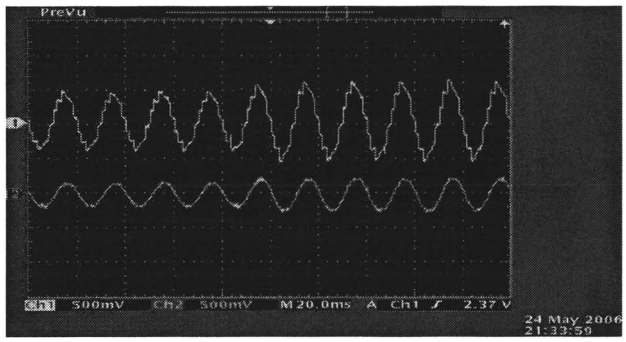

Figure 11: The Load phase voltage v_{aN} and the line current i_a (150V/ div, 5Amp/ div, 20ms/ div).

5 Conclusions

This paper presents a three-phase three-level nine switch voltage source inverter, where an additional auxiliary circuit which consists of three bi-directional switches has been inserted between the source and the full-bridge power switches of the classical three-phase inverter. As a result, a significant reduction of the load harmonics contents is obtained at the inverter output. Its operating principles, analytical, and switches timing chart based on harmonic minimization control scheme are analyzed in details. A prototype has been designed; implemented and tested; also the PID controller has been designed and implemented in the case of a step change in the inverter DC bus voltage. The dynamic responses of load waveforms due to the step change are provided. The simulation and experimental results show that THD of the proposed inverter is considerably improved.

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