Three-Phase Three-Level Nine Switches Inverter Employing Space Vector Modulation

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***Abstract*— This paper studies the space vector pulse width modulation technique (SVPWM) for the three-phase three-level nine switches voltage source inverter. The proposed inverter is based on the two level inverter topology where it consists of a main inverter switches Q_1, Q_2, Q_3, Q_4, Q_5, and Q_6, an auxiliary three bidirectional switches S_1, S_2, and S_3 and two capacitor banks C_1, and C_2. Ideal switches and diodes will be assumed and the dc bus capacitor bank voltages fluctuations will be absent. The effectiveness of the SVPWM control scheme will be verified by the simulations results in the worst case where two very low switching frequencies values of 1 kHz and 5 kHz will be considered. Open loop controller experimental measurements at 1 kHz switching frequency will be provided.**

***Index Terms*— two level inverter, three-phase three-level inverter, space vector pulse width modulation**

I. INTRODUCTION

Figure 1 shows a three-phase three-level inverter topology based on the two-level inverter topology which has been proposed in [1]. Switches Q_1, Q_2, Q_3, Q_4, Q_5, and Q_6 represent the two-level inverter topology besides bidirectional switches S_1, S_2, and S_3 represent an auxiliary circuit. It employs a simple control scheme at low switching frequency due to that the selected harmonic elimination technique (SHE) has been chosen to generate switches pulses required for optimum operation or lowest voltage output total harmonic distortion (THD). It has been found that switches Q_1, Q_2, Q_3, Q_4, Q_5, and Q_6 operate at main line power frequency, while bidirectional switches S_1, S_2, and S_3 operate at twice main line power frequency. The main line power frequency is chosen at 50 Hz. Such a way of creating output waveforms has some advantages: simple control circuitry besides operation at low switching frequency make the problem of both electromagnetic interference (EMI) and devices voltage stress to be nearly absent. The main disadvantage of such a control method is a high harmonic content of the output voltage-THD amounts to 15.5% which needs extra filter which increases the complexity of the layout circuit and the component used.

With the introduction of multi-level voltage-source converters [2], various modulation techniques have been developed for pulse width modulation (PWM). PWM has been studied extensively during the past decades. Many different PWM methods have been developed to achieve less THD, easy implementation and less computation time. With the development of microprocessors, space-vector modulation (SVM) has become one of the most important PWM methods for three-phase converters [3]–[6]. It uses the space-vector concept to compute the duty cycle of the switches and it is simply the digital implementation of PWM modulators.

The paper will start in section II with explaining the block diagram of the proposed inverter, and the analysis of the SVM for the three-level inverter. Section III subsequently presents the SVM algorithm for the three-level nine switches inverter. Serving as a reference for inverter validity, section IV gives Matlab simulated results which are used for verifying the performance of the proposed design procedure whose analysis is presented in Section II for the three-level nine switches inverter. Last, Section V summarizes the conclusion presented in the paper.

II. SPACE VECTOR MODULATION FOR THREE-LEVEL INVERTERS:

The schematic diagram of the three-phase three-level nine switches voltage source inverter is shown in Figure 1. It consists of three-phase three-level nine switches voltage source inverter and its control circuit. For simplicity, inverter switches and diodes are assumed to be ideal; in addition, inverter dc bus capacitor bank voltages fluctuations will be absent. Turning on one of the upper switches Q_1 or Q_3 or Q_5 will produce output voltage level equals ($2\ V_{dc}$) for v_{an} or v_{bn} or v_{cn} respectively, while turning on one of the bottom switches Q_2 or Q_4 or Q_6 will produce voltage level equals zero for v_{an} or v_{bn} or v_{cn} respectively, and turning on one of the bidirectional switches S_1 or S_2 or S_3 will produce voltage level equals (V_{dc}) for v_{an} or v_{bn} or v_{cn} respectively. Generally every

switching state produces specific three-phase voltages v_{an}, v_{bn}, and v_{cn} referred to the neutral of the dc bus voltage which can be defined as follows:

$$\begin{aligned} v_{an} &= k_a V_{dc} \\ v_{bn} &= k_b V_{dc} \\ v_{cn} &= k_c V_{dc} \end{aligned} \quad (1)$$

Where k_a, k_b, and $k_c \in [0, 1, 2]$, and switching states of line-to-line voltages are governed by the following equation.

$$\begin{aligned} v_{ab} &= v_{an} - v_{bn} = (ka-kb)\ V_{dc} \\ v_{bc} &= v_{bn} - v_{cn} = (kb-kc)\ V_{dc} \\ v_{ca} &= v_{cn} - v_{an} = (kc-ka)\ V_{dc} \end{aligned} \quad (2)$$

Equation (2) can be put in matrix form as follows

$$V_{l-l(ka,b,c)} = V_{dc} \cdot [\, k_a - k_b \quad k_b - k_c \quad k_c - k_a \,]^T \quad (3)$$

Similarly, a reference line-to-line voltage vector in steady state can also be represented in vector form

$$V_{REF} = V_{l-l} \cdot [\cos(\omega t) \quad \cos(\omega t - 2\pi/2) \quad \cos(\omega t + 2\pi/2)]^T \quad (4)$$

Representing both of $V_{(ka,b,c)}$ and V_{REF} defined by equation (3) and (4) in d-q stationary plane by using the following transformation:

$$\begin{aligned} V^*_{l-l(ka,b,c)} &= [\,1 \quad e^{j\frac{2\pi}{3}} \quad e^{j\frac{4\pi}{3}}\,] \cdot V_{(ka,b,c)} \\ V^*_{REF} &= [\,1 \quad e^{j\frac{2\pi}{3}} \quad e^{j\frac{4\pi}{3}}\,] \cdot V_{REF} \end{aligned} \quad (5)$$

Figure 2 shows all the switching vectors of a three-level (n = 3) multilevel inverter labeled with the position of the equivalent phase switches defined by the first part of equation (5). Note that the reference voltage vector V^*_{REF} is represented by a circle; the radius of this circ le is defined by $\left|V^*_{REF}\right|$.

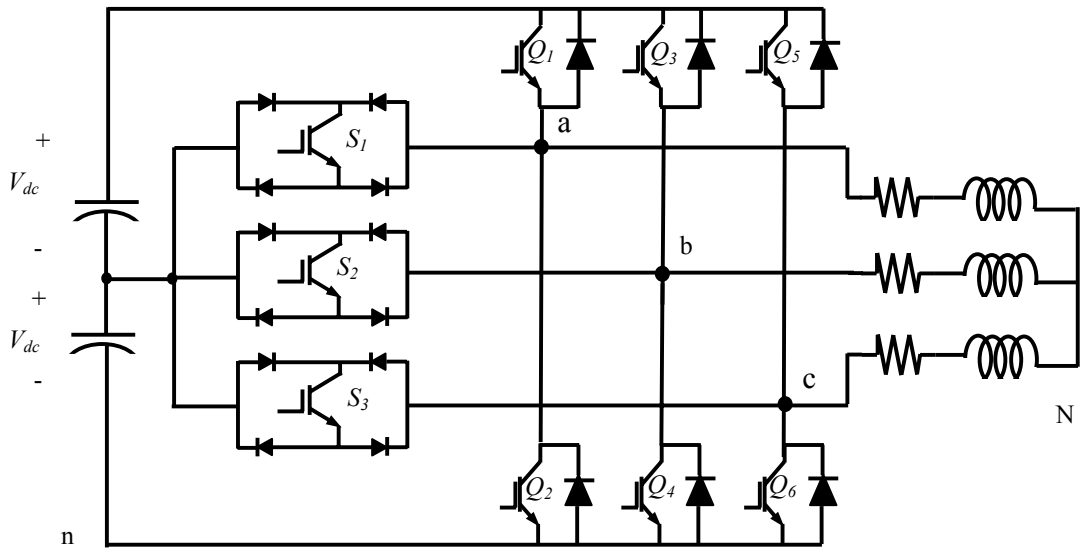

Figure 1: The proposed three-phase three-level nine switches inverter

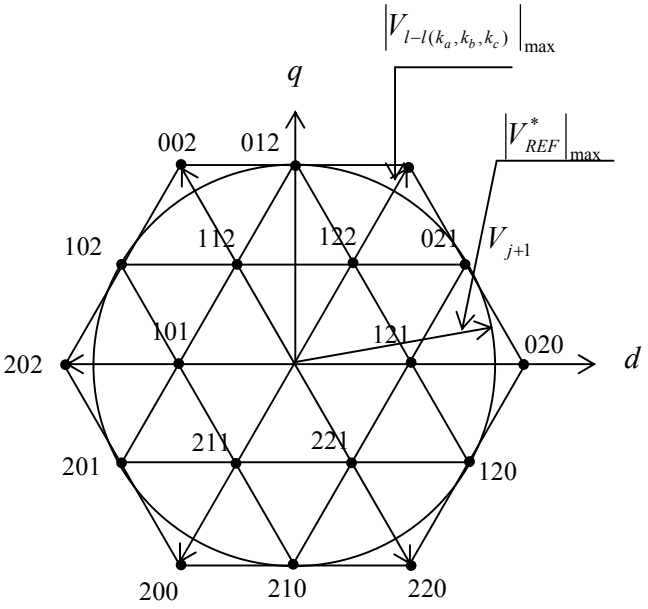

Figure 2: Switching states of a three-level inverter

Figure 3 illustrates the MALAB SIMULINK propgram to execute the aformentioned analysis that can generate switches states for inverter switches.

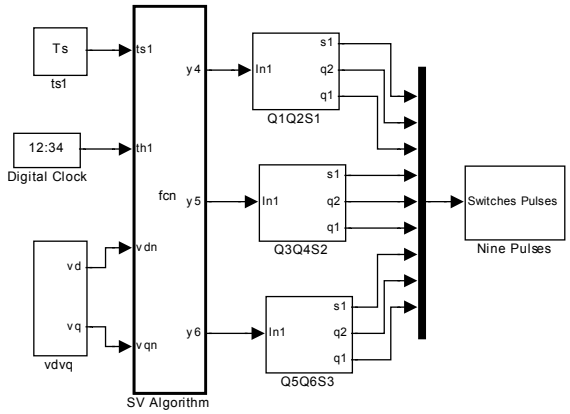

Figure 3: MATLAB/SIMULINK program to execute switches states

III. The Space Vector Modulation Algorithm for 3-Levels Inverter

Based on algorthims explained in [7-8], switches ON/OFF states can be evaluated, the following steps summarizes this procedure.

- First step is the normalization of the reference line-to-line space vector voltage as follows [7]:

$$(V_{REF})_{\text{nor}} = (n-1)\frac{V_{REF}}{V_{dc}}$$

This normalization depends on the number of levels of the multilevel inverter n and the voltage level value of the dc bus capacitors V_{dc}.

- Locating the region of the reference line-to-line refernce space vector, calculating the three nearest line-to-line switching voltages v_{an} v_{bn}, and v_{cn}, and their switching times are the second step [8].

Having evaluated v_{an} v_{bn}, and v_{cn},, therefore k_a, k_b, and k_c, and hence switches on/off state can be derived as follows for phase a:

$$k_a = \begin{cases} 2 & Q_1 \text{ ON otherwise it is OFF} \\ 1 & S_1 \text{ ON otherwise it is OFF} \\ 0 & Q_2 \text{ ON otherwise it is OFF} \end{cases}$$

IV. Simulation Results

Simulations have been carried out for two values of switching frequencies 1 kHz and 5 kHz. For better comparison; simulations results of the proposed inverter are compared with previous results for the normal three-level inverter [8]. To do so, the considered operation conditions are: the dc capacitor voltage V_{dc} = 120V and R-L load. Where R = 20Ω and L = 5mH.

Figure 4 to Figure 7 illustrate output simulation results in case of 1 kHz switching frequency. These results are organized as follows; normalized line-to-line inverter output voltages $V_{ab,}$ V_{bc}, and V_{ca} ; normalized three-phase output voltages referred to the dc link V_{an}, V_{bn}, and V_{cn}; line currents i_a, i_b, and i_c; and the harmonic contents of the line current reprented by THD respectively.

Similarly simulation results for 5 kHz switching frequncy of normalized line-to-line inverter output voltages $V_{ab,}$ V_{bc}, and V_{ca} ; normalized three-phase output voltages referred to the dc link V_{an}, V_{bn}, and V_{cn}; line currents i_a, i_b, and i_c; and the harmonic contents of the line current reprented by THD as shown by Figure 8 through Figure 11 respectively.

Note that choosing operatation at low swicthing frequency represents the worst case where it is accompanied by injection much harmonics in the output, and the higher the swicthing frequency is employed the lower the harmonics contents in the output is produced.

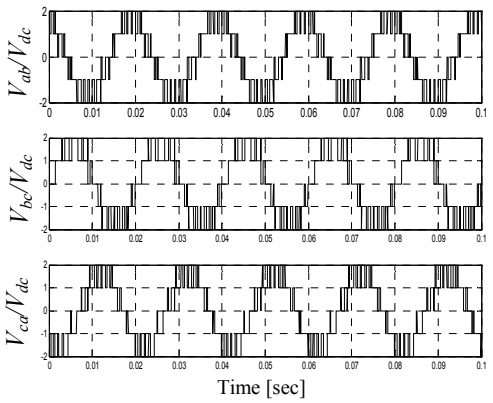

Figure 4: Normalized line-to-line voltages at 1 kHz switching frequency

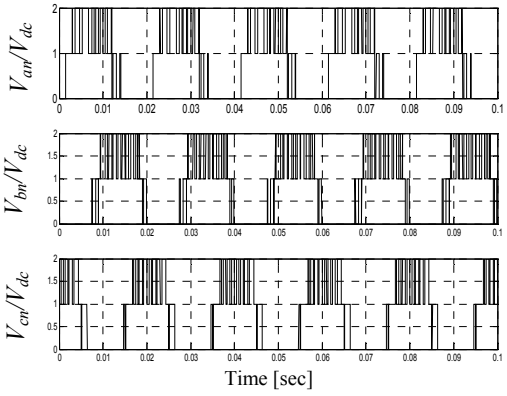

Figure 5: Normalized three-phase inverter output voltages referred to the neutral of the dc bus link V_{an}, V_{bn}, and V_{cn}.

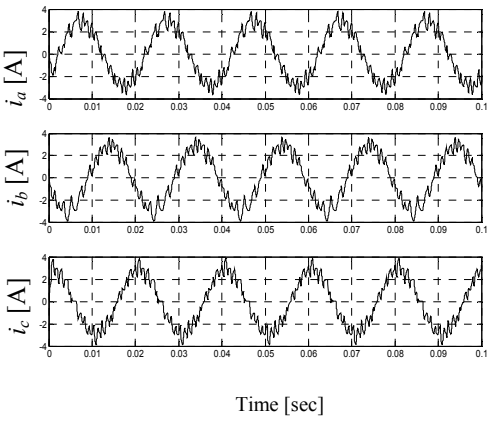

Figure 6: Load line currents i_a, i_b, and i_c at 1 kHz switching frequency.

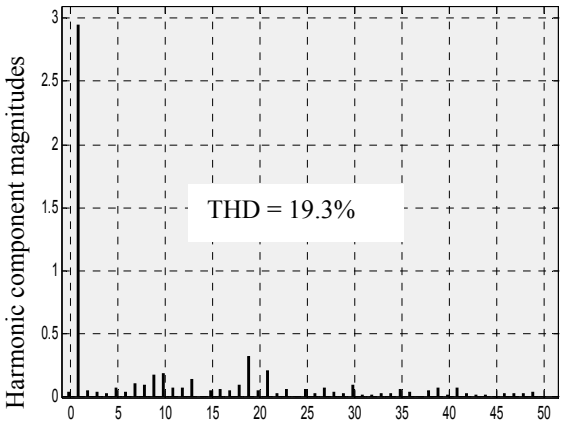

Figure 7: THD for the load current for 1 kHz switching frequency

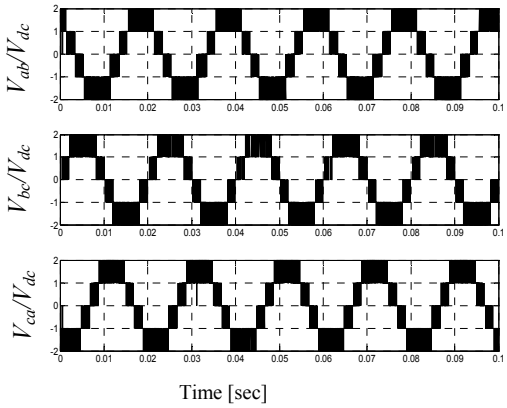

Figure 8: Normalized line-to-line voltages at 5 kHz switching frequency

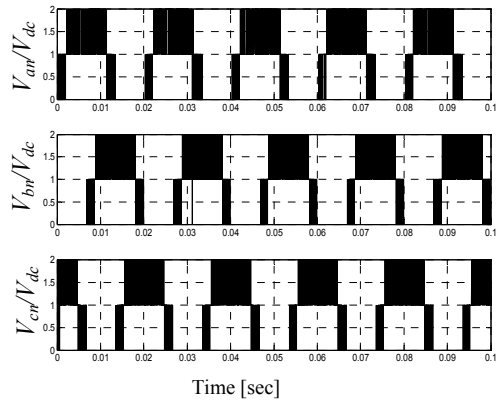

Figure 9: Normalized three-phase inverter output voltages referred to the neutral of the dc bus link V_{an}, V_{bn}, and V_{cn}.

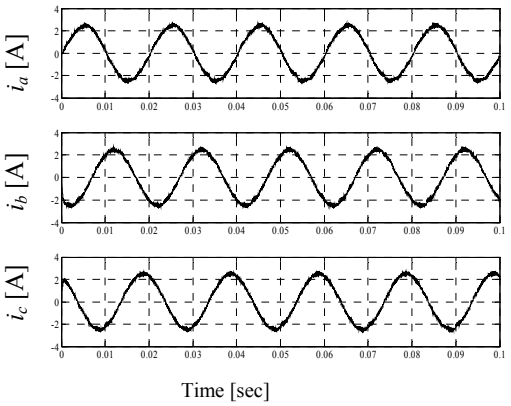

Figure 10: Load line currents i_a, i_b, and i_c at 5 kHz switching frequency.

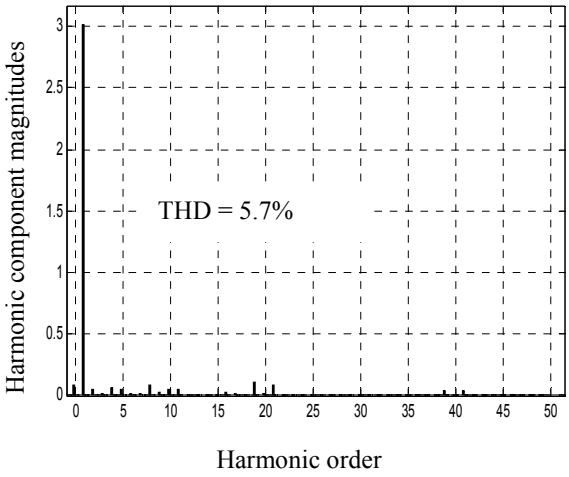

Figure 11: THD for the load current for 5 kHz switching frequency

V. LABORATORIES MEASUREMENTS

The experiments were conducted using open-loop controller and the input DC inverter bus voltages are assumed to be fixed without fluctuations. A DSP TMS320F2812 board has been as a controller. Switches pulses generation program shown in Figure 3 runs in MATLAB and its results are downloaded and stored in the DSP board. Due to the speed limitations of the controller, results have been carried out only for the lowest switching frequency which is 1 kHz. the considered operation conditions are: each dc capacitor voltage V_{dc} = 60V , thus 120V on the inverter dc bus, static R-L load with R = 20Ω and L = 5mH, and fs = 1 kHz.

Figure 12 illustrates controlling pulses of inverter switches, for phase a, generated by DSP TMS320F2812 controller using the aforementioned procedure at 1 kHz switching frequency.
Figure 13 illustrates the line-to-line voltage of V_{ab} and V_{ca} respectively, with 240V peak-to-peak and about 75V RMS. Figure 14 shows load phase voltages v_{an}, v_{bn}, and v_{cn} referred to the neutral of the DC bus voltage.

Figure 15 shows the line currents i_a, and i_b, while Figure 16 shows the line currents i_b, and i_c. The output current harmonic contents at switching frequency 1 kHz is shown in figure 17.
The simulation results and the laboratory measurements verify the effectiveness of the SVPWM control scheme for the proposed inverter

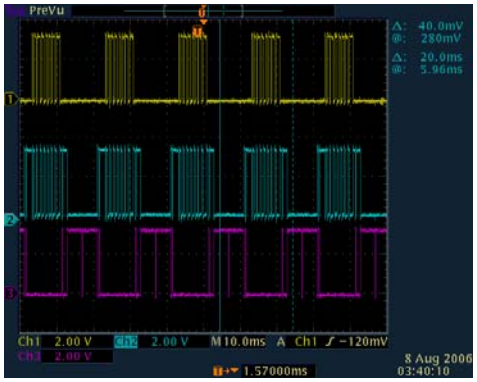

Figure 12: controlling pulses of Q_1, S_1, and Q_2 switches respectively at 1 kHz switching frequency.

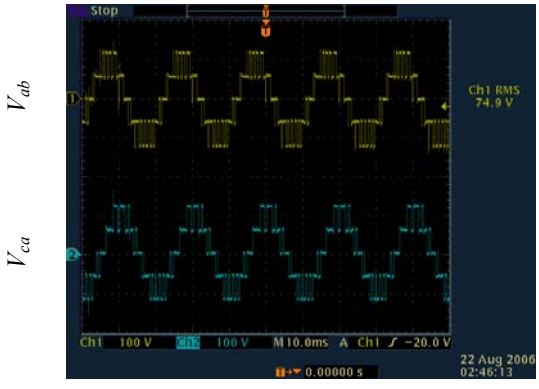

Figure 13 Line-to-line voltages V_{ab} and V_{bc} at 1 kHz switching frequency (10msec/div, 100V/div).

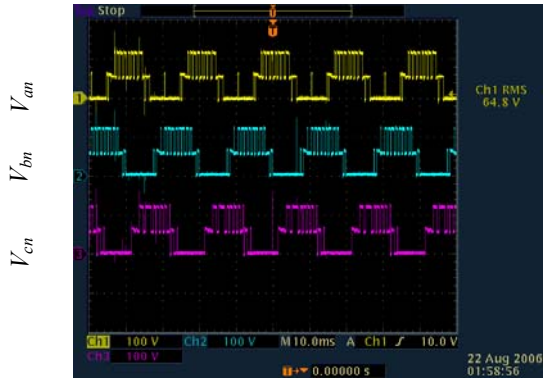

Figure 14 Experimental results of the three-phase inverter output voltages referred to the neutral of the dc bus link V_{an}, V_{bn}, and V_{cn}. (10msec/div, 100V/div).

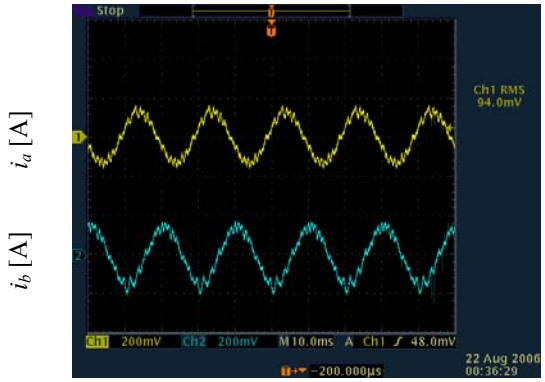

Figure 15 Experimental results of the load line currents i_a, i_b (10msec/div, 4A/div)

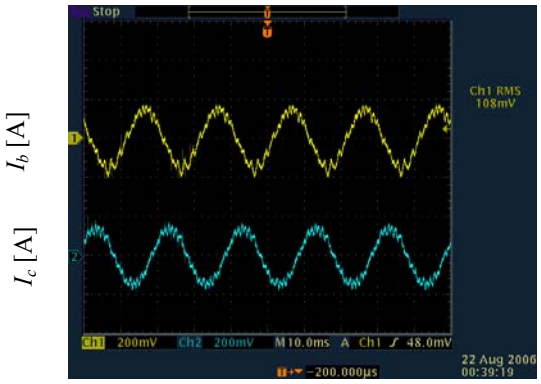

Figure 16 Experimental results of the load line currents i_b, i_c (10msec/div, 4A/div)

VI. CONCLUSION

The performance of the three-phase three-level nine switches inverter proposed in [1] has been improved in this paper by employing SVPWM control scheme. The simulation results have been provided for the worst case of operations where the switching frequency has been chosen very low 1 kHz and 5 kHz. The THD has been found 19.5% and 5.5% at 1 kHz and 5 kHz switching frequencies respectively; where the higher the swicthing frequency is employed the lower the harmonics contents in the output is produced. Open loop controller experimental measurements at 1 kHz switching frequency have been provided. The simulation results and the laboratory measurements verify the effectiveness of the SVPWM control scheme for the proposed inverter

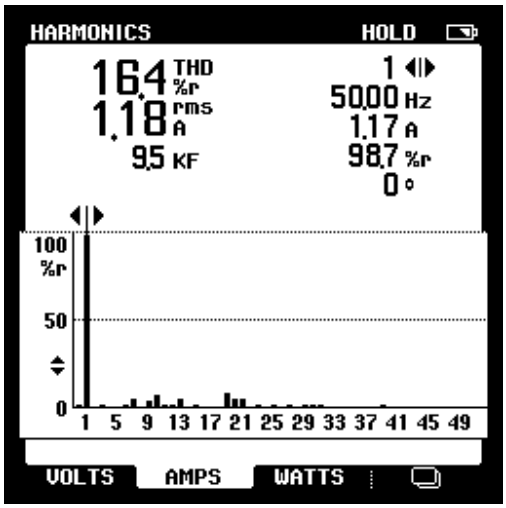

Figure 17: Harmonic current spectra for 1 kHz switching frequency.

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