Buck and Boost Converter Design Optimization Parameters in Modern VLSI Technology

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***Abstract* – This paper presents the feasibility challenges of designing dc-dc buck and boost converter in nano-scale. With the gradual development of VLSI design platforms, new issues have been introduced and presented to the power electronics circuit experts and VLSI engineers. Today's VLSI industry has reached the technology well within the nano-meter range. The consequence of implementing the basic power electronics converter topology such as buck and boost converter into this technology is discussed in this paper. It also covers the optimization issues between conduction modes, switching frequencies, efficiency and chip area. Fabrication issues are discussed, with the limitations of use of elements such as inductor, capacitors and resistors. Tradeoffs between chip area and performance are highlighted. Design challenge for optimum switching frequency, off the chip capacitor, and strategies to minimize switching and conduction losses are also discussed**

***Index Terms* – Dc-Dc Buck, Boost converter, VLSI design, Efficiency, Switching frequency**

I. INTRODUCTION

THE INSERTION OF BASIC dc-dc converter such as buck and boost, in VLSI layout has several implications. Firstly, the amount of dissipated power. Realistically only a small amount of power can be converted (less than 1W). Secondly, the power density is very high. A way to resolve the second problem is to use high speed MOSFET switches operable in very high frequency (above 1 MHz) therefore reduce the area for the passive components. The passive components comprise the majority of the chip area [1]. The MOSFET switches occupy smaller area, which is one of the much desired features for the VLSI engineers. The condition that constraints the number of MOSFETs is the stray capacitance and switch ON/OFF state current/voltage handling capability. The development of microprocessor performance was based on the three factors. 1: MOS transistor speed, 2: Clock frequency increase and 3: Architecture improvement. Ever since the year 2000, the clock frequency has become more or less stall because of overheating chip. Also the miniaturization of MOS transistors has become saturated due to the power dissipated in form of heat. The only way remaining to improve the chip performance is by working on the architecture. Nevertheless only improvement in architecture is not enough for the whole device performance [2]. Dc-Dc power converters are necessary to change the appropriate voltage and current levels based on the need of the particular application. The increasing miniaturization leads to portable, wireless and battery operated applications. The battery voltage is however much too high for some parts of the sub-micron circuits therefore it needs to be decreased. Conventional linear regulator for this task will lead to extensive heat loss, whereas switch mode power converter can convert the voltage levels and increase lifetime of the battery. The reason switched mode converters supersedes linear regulator is the efficiency. SMPS (switched mode power systems) are highly efficient [3]. Advanced semiconductor technology continues to push the device sizes into the nanodimensional regime. Current research progress in VLSI industry theoretically is making MOSFET dimensions push towards the 10nm gate limit. However in such a small area of analysis cannot be done using only the deterministic approach. Because the natural limit of certainty and probability will be violated and quantum effects of particle will take over [4]. Quantum effects and non deterministic physics are out of scope for this paper therefore fabrication process that ranges from 350-90nm- are only considered for this paper.

II. FABRICATION HISTORY

Since the 1990s silicon based CMOS (complementary metal oxide semiconductor) obtained steady advancement with miniaturization and low power consumption. The development of semiconductor technologies commenced rapidly with the increased superiority of CMOS fabrication process. For example: the revolutionary improvement in applications such as microprocessor for PCs, server and router for internet applications, RF for cellular phones, analog circuitry, wireless LAN technology and many more. Fabrication process had entered the "nano" region almost ten years ago (2000) with the technology of 130 nm [5]. Current research and literature show that by the end of year 2015, it is estimated to achieve the minimum channel length as the unit of fabrication process which is also the natural limit of the CMOS, around 10nm. Beyond this, the deterministic approach of analysis will not become valid anymore.

A. Fabrication Limitations for Converters

Most integrated circuits are constructed with CMOS technology. The key factors in determining the cost of a CMOS circuit are the following: 1) Size, 2) Number of components and layers, and 3) Total chip area occupied.

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CMOS process enables the option to design in multilevel and multi layered placement of elements such as inductors, resistors and switches. Components that are necessary for energy storage such as inductor and capacitor, occupy a significant amount of space. The reason why dc-dc low power converters are feasible in CMOS process is because of the CMOS switches. The transistors can easily block up to 15 volts which is highly desirable for dc-dc buck and boost converter operation.

III. DC-DC BUCK AND BOOST CONVERTER OPERATIONS

The basic converter topology is the buck and boost converter. Buck converter has the ability to provide reduced voltage and boost converter provides increased voltage. Both the converters operate based on the inductor volts-second balance and capacitor amp-second balance. Dc-Dc converters are highly efficient compared to the traditional linear regulators. The basic converter includes, MOS switches, inductor, capacitor and resistor. For a typical boost converter operating 3V-6V, 1W, requires the inductor to carry current around 300 mA [6]. For an inductor to be able to handle this much current, the layout needs to be at least 300µm width (1µm per 1mA). Usually the insertion of spiral inductor is an option to achieve the size and the value of inductors. Also to ensure the converter operates in CCM (continuous conduction mode) the used inductor must be higher than the critical inductance (L_{crit}) of the converter.

A. Switching Frequency and Optimization

At higher switching frequency, the switching losses become dominant and at lower switching frequency the conduction loss such as skin effect and resistive loss will dominate. For efficient energy storage operation, it is desirable to have a high quality factor for the inductor, but the inductor quality factor is directly proportional to the applied frequency.

$$Q_L = (2\pi fL)/R_L \quad (1)$$

where
Q_L is the quality factor
L is the inductance (fixed)
R_L is the load resistance (fixed)
f is the applied frequency

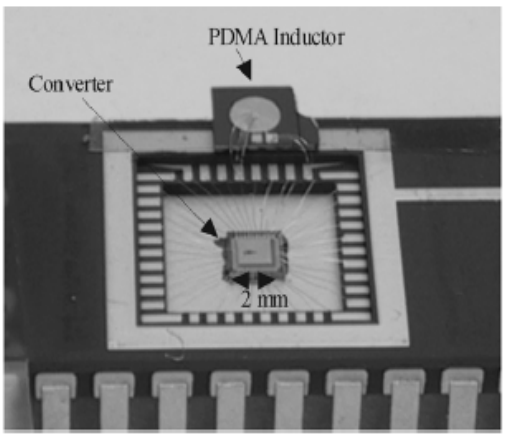

Fig1: PDMA (plastic deformation magnetic assembly) [11]

The biggest limitation of spiral inductor is poor quality factor. So the tradeoff is to choose between cost-space and quality in the inductor design based on the application. For applications which requires power level less than 0.1W, converters need to be designed to operate higher than 20 MHz, and the inductor trace width around 100 µm [6]. However, if the power requirement is high then additional complexity arises in the design. If the required power is around 0.5 W–1 W, then the operating frequency can be used well above 15 MHz [6]. This is an optimum switching frequency for high Q and moderate switching loss. Researchers have shown that very high switching frequency such that of the order of 8 0MHz is capable of maintaining a very high efficiency, but at such a high frequency the device life, EMI, stress on the CMOS, become dominant in the long run. Moreover, 233 MHz operating converter with 80% efficiency have been reported operational but the inductor design has been external (On-Package) [7]. Also the conversion voltage is below 1 V. So it is clearly noticeable that high power requires more inductor area, and higher switching frequency is required for efficient operation of the inductor/converter. In recent research PDMA, see Fig 1 (plastic deformation magnetic assembly) has been reported as a successful technique to design on package [8].

IV. MOS SWITCHES AND OTHER PARAMETERS

The specific channel width and length are set according to the designer's preference. The layout diagram is constant but the channel width remains a design variable as it is known that the width of the MOS gate is a measure of the current handling capability. Channel length is also chosen to minimize the resistive loss and the width of the metal trace is to be selected based on the average switch current.

A. Optimizing Resistance and Capacitance

Among other considerations to design the MOS switches, the most important of them is the estimation of parasitic resistance and capacitances. Among the parasitic resistances the most significant ones are such as lead resistance, contact resistance, channel resistance, gate resistance etc. Superior device selection, careful modeling and special fabrication process technology such as DMOS [9] can be implemented to eliminate or ignore most of the resistive losses except the contact resistance which is an internal property of the metal-CMOS contacts used in different layers of the converter. Also the increased width of the gate, give a rise to the gate resistance and therefore increased conduction loss. The factor which determines the value of the parasitic resistance is the cut off frequency of the inductor and the amount of current that it has to carry.

Also the channel resistance is heavily dependent on the fabrication process because it involves the use of electron mobility µ and gate oxide capacitance C_{ox}. As a design strategy, the width of the transistor can be assumed to be

twice the width of the metal trace used to fabricate. So a designer's estimate for the total area of the chip would be such as following:

$$\text{Area} = N_t * W * L \quad (2)$$

where:

N_t is Number of transistors in a chip

W is channel width

L is channel length

It is noted that the width of the metal trace is proportional to the intended current carrying ability. As a designer's rule of thumb, every 1μA of metal trace is capable of carrying 1mA of current [13]. Therefore this is the bottom line for the tradeoff between cost/size, and power rating of the CMOS converter.

The highly "non-desired" element in fast digital circuits i.e. capacitors, are very much desired in CMOS VLSI converter design. The major problem about the parasitic capacitance is they are not predictable. The common parasitic are gate to drain, drain to body and gate to source capacitance. The gate capacitance can be expressed as follows:

$$C_g = C_{ox}\, w_t \quad (3)$$

where

C_g is the gate capacitance

C_{ox} is the SiO2 capacitance

W_t is the width of the channel

From equation (3) it is clearly visible the wider the channel is the more parasitic gate capacitance is going to be produced. So this is one major optimization issue for the designer to choose between functionality and device fabrication cost because device with higher width will cost much more in a fabrication process.

Based on the literatures reviewed and current findings of this area, the table is summarized below in order to assist the designers to choose among the variables:

TABLE 1
COMPARISON OF CONVERTER DESIGN PARAMETERS AND EFFECTS

No	Parameter	Perturbation	Parasitic (resistance /capacitance)	Cost	Power handling	Loss	Ripple	Efficiency	Mode of Conduction
1	Switching Frequency	Increase	Decrease	high	low	high	low	high	CCM
		Decrease	Increase	high	high	low	high	low	DCM
2	Inductance	Increase	Increase	high	high	high	high	N/A	CCM
		Decrease	Decrease	low	low	low	low	N/A	DCM
3	Capacitance	Increase	Increase	low	N/A	high	low	low	CCM
		Decrease	Decrease	high	N/A	low	high	N/A	DCM
4	Resistance	Increase	Increase	high	high	high	high	low	CCM/DCM
		Decrease	Decrease	low	low	low	low	high	DCM/Non Operational
5	Chip Area	Increase	Increase	high	high	high	N/A	low	CCM/DCM
		Decrease	Decrease	low	low	low	N/A	high	CCM/DCM
5	Chip Layer	Increase	Increase	high	high	high	N/A	low	CCM/DCM
		Decrease	Decrease	low	low	low	N/A	high	CCM/DCM

V. CONCLUSION

Minimization of the chip area occupied by fully integrated CMOS dc-dc buck and boost converter is important ultimately in order to reduce the cost for production. Different approaches for designers were discussed based on the device requirement. The size of the buck and boost converter MOS switches have been comprehensively studied throughout the paper. This paper is intended to act as a guideline for future designer in the field of power electronics engineering and VLSI designers. We look forward to concentrate on each of the methods to resolve the further issues addressed in this paper to design CMOS dc-dc buck and boost converter. Future work will heavily concentrate on such design and verification and optimization of converter parameters using the VLSI design platform.

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