Three Phase Hybrid Multilevel Inverter Control Using Vector Transformation

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ABSTRACT

This paper presents a multilevel multistage inverter design and its corresponding control strategy. The hybrid inverter has a high voltage stage composed of the six-switch conventional three phase inverter with its output connected in series with the outputs of three-level H-bridge medium and low voltage stages. The voltage ratio has been selected to enable both one state - approximation and PWM control modes effectively. The suggested control strategy has been developed to ensure minimum switching losses focusing on holding the higher voltage stage state as long as it is feasible. The reference voltage vector has been approximated to the nearest of the 919 vectors provided by the 18-level inverter. A special definition of state zone has been introduced for the low voltage stage to enable the achievement of the reference vector with minimum error. The proposed control strategy has been tested and its short computational time and low memory requirement has been proven.

Index Terms— Converters, multilevel inverters, DSP control, pulse width modulation.

1. INTRODUCTION

Multilevel inverters have been introduced to enable the construction of inverters of voltage ratings beyond the switching devices capability. Other advantages of this type of inverters are the ability to produce less distorted waveforms and the reduced dv/dt in its output. The basic multilevel inverter topologies which are the neutral point clamped, flying capacitors and the series connected H-cells enable the construction of inverters with any number of levels theoretically. Due to the increased circuit complexity, number of series connected devices and cost, the number of levels of practical multilevel inverters with the basic topologies is very limited. Modifications have been introduced on the basic topologies. The number of levels of the symmetrical multilevel inverter is linearly proportional to the number of devices. The asymmetrical multilevel inverter obtained by supplying various input ports with different voltages can have a number of levels exponentially proportional to the number of devices. Therefore this choice has been adopted by many studies. The design of the inverter can be further optimized by hybridization, where the multilevel inverter is constructed from inverter stages of different types, topologies and/or voltage levels. Asymmetrical multilevel inverter has been obtained in various ways. The cascaded H-bridge cells topology is the most common due to its modular structure and simple circuit. Among the first reports is the combination of two H-bridge inverters fed with different DC input voltages. It has been shown that when the DC voltages are related by the ratio of 1:3 the maximum output resolution, i.e. number of levels, can be obtained [1]. The voltage ratio selection rules have been identified in following studies [2], [3] which introduced two conditions for voltage ratios selection; the uniformity of the steps and the modulation condition. The uniformity of the steps is insured if the inverter output voltage levels are evenly spaced. While the modulation condition is satisfied if any two adjacent levels can be achieved by changing the switching state of the lowest voltage inverter only and holding the state of the higher voltage cells. The last condition meant to ensure no high switching frequency at the high voltage stage. Some studies [4-6] did not consider the condition of the modulation instead the number of levels has been maximized by selecting input voltages of the two or three- stage inverters related by ratio 3. In all these studies, the carrier-based or the space vector PWM control have not been considered, instead selected harmonics elimination [4] or the one switching state per sampling interval [6] has been adopted assuming that the inverter high resolution can ease the need for PWM control. The desirable characteristics of hybrid multilevel inverter can be summarized by: i. High number of levels –to–switching devices ratio. ii. Capability of effective PWM control. iii. Low cost of the DC supplies circuit. iv. Good utilization of the inverter elements. The asymmetrical multilevel inverter of ratio-3 fed cascaded inverter provides the highest number of levels-to-circuit elements ratio but this design requires high number of isolated DC supplies making DC supply circuit rather complicated, costly and operating with highly reactive current. Also PWM control of this inverter leads to high switching frequency of the high voltage stage.

This paper presents a modification of the ratio-3 supplied asymmetrical multilevel inverter by replacing the higher voltage stage of three single-phase H-bridge inverters by a three-phase six switch inverter. This arrangement has been used in the two-stage, 6-level inverter topology presented in

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[7]. A novel one state per sampling interval control algorithm has been developed and presented.

2. INVERTER STRUCTURE, VOLTAGE VECTORS AND SWITCHING STATES

The cascaded H-bridges inverter has the disadvantage of expensive dc sourcing. For a 3-stage inverter nine isolated dc supplies are required. These supplies operate with high reactive power and peak-to-average current ratio. In the proposed design, the high voltage three H-bridge inverters have been replaced by one six switch three phase inverter; this reduces the number of high voltage supplies to one and the reactive power requirement for this stage, and hence the cost and losses of dc sourcing. The inverter, as shown in Fig. 1, is composed of the "main" high voltage six-switch inverter with each output line connected in series to two cascaded single-phase full bridge inverters. The main and H-bridge cells are fed by isolated dc sources of a different values related by the ratio 3. The justification of this voltage ratio is presented in the following subsection.

2.1. The Voltage Vectors and Inverter States

The voltage vectors of the three-stage inverter can be determined graphically by superimposing the vector diagram corresponding to three stages. The full vector diagram can be achieved by positioning vectors corresponding to medium stage at the tip of each of the seven vectors corresponding to high voltage stage. Then, to include the effect of the low voltage stage, the low voltage vectors are added at the tip of the medium voltage vectors. The resultant vector diagram, with the voltage ratios indicated in Fig.1, is shown in Fig. 2. Fig.2 shows the virtues of ratio-3 selection which are besides the evenly spaced 18-level inverter vectors, the capability for PWM operation without high frequency switching of the high and medium stages. Where almost any voltage vector located in the grand hexagon of Fig. 2 is located inside one of the smallest hexagons formed by the low voltage stage vectors. Therefore any reference vector can be achieved by fixing the high and medium stages states and operate the low voltage stage to produce the three vectors nearest the reference vector with suitable duty ratios in a way similar to that given in [8].

It is highly desirable for the switching frequency of the high voltage inverter to be minimized. The control algorithm explained in the next section aims to hold the high voltage vector as long as the reference vector can reached through this high voltage vector. We will refer to the hexagonal area marked by the vectors reachable through a given high state vector by its domain.

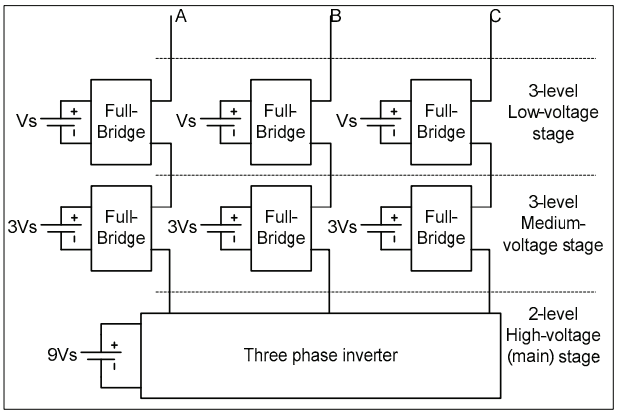


Fig. 1. 18-level inverter topology

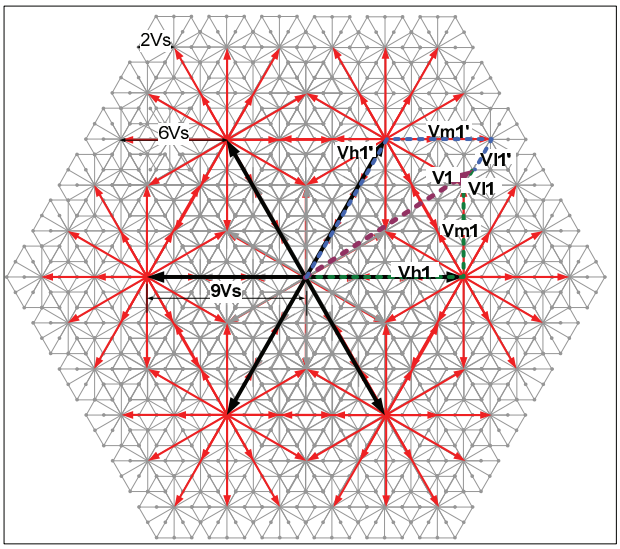


Fig. 2: The voltage vectors of the 18-level inverter as the sum of the three cascaded inverters vectors

3. THE CONTROL STRATEGY

The flow diagram of the control algorithm is shown in Fig. 4. The controller checks if the reference voltage vector, to be realized in the next sampling interval, is located in the domain of the current high voltage stage vector. If so the inverter will hold the high voltage stage state otherwise it will replace it with the nearest state. The nearest state is defined as the state that can be reached with minimum number of the switching actions and has the reference vector in its domain. After selecting the high voltage inverter state, its corresponding voltage vector is subtracted from the reference vector results the middle reference to be realized by the middle and low voltage stages. The middle reference vector is compared to the current middle state domain. If the middle reference is located within its domain the current middle state will be held, otherwise it will be change by the nearest state. Low voltage stage reference is

determined by subtracting the voltage vector corresponding to the next middle state from the middle reference. The low voltage stage simply outputs the nearest voltage vector with minimum switching transitions.

4. IMPLEMENTATION

The control algorithm explained in the past section has been implemented by the controller board eZdsp F2812. The 150MHz, fixed point, low cost CPU, ran the algorithm with a sampling frequency acceding 25kHz and using the on-chip memory only reflecting the computational efficiency of the control algorithm.

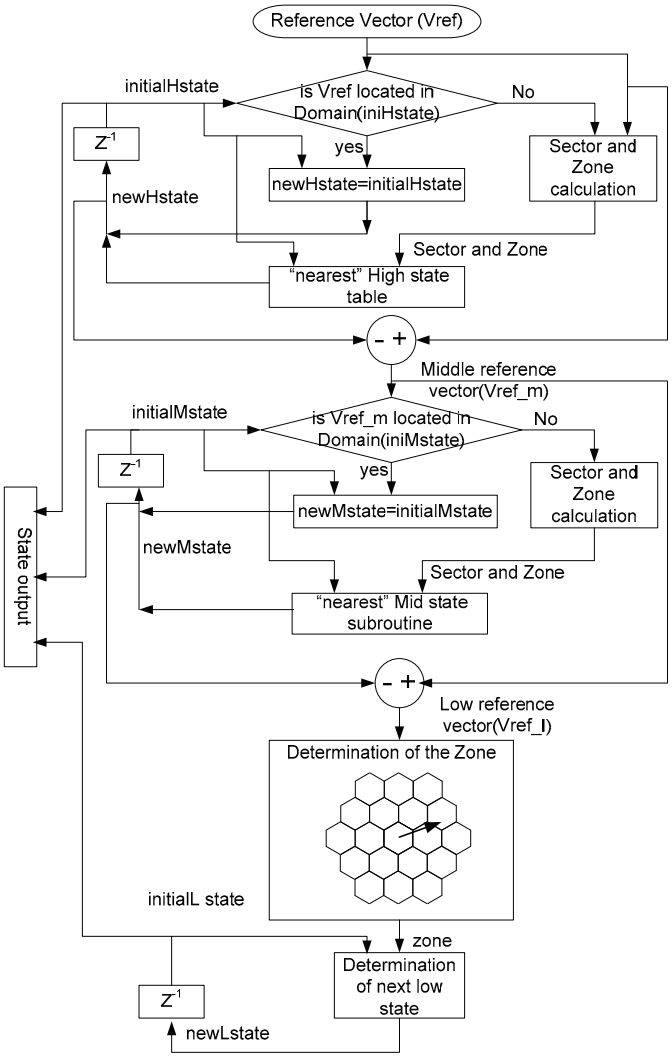


Fig. 3: Flow diagram of the 18 level inverter control algorithm

A 16-bit input port has been allocated for the reference input. The 8 MSBs have been regarded as the reference voltage amplitude where the step dc voltage (Vs) is assumed to be equivalent to (10)16. The maximum reference amplitude (FF)16 has been set to be corresponding to a reference amplitude of almost 16Vs. This limit is justified by the fact the maximum norm of reference vector that is certain to be within the hexagon must be less than 15.588Vs. Although the resolution of this representation is 1.875°/bit and this is not the maximum resolution permitted by the 8-bit representation but this system allows direct determination of the operating sector as the 3 MSBs of the angle byte which saves computational time. On the other hand, the minimum angle between any two adjacent voltage vectors of the 18-level inverter is about 2.83°.

5. RESULTS

The suggested inverter circuit and the control algorithm have been simulated to verify their validity. With a reference sinusoidal of 50Hz and magnitude control ratio of 80%, the resultant switching signals of the three stages as well as the load phase voltage waveform are shown in Fig. 4. The results show that the high voltage stage basically operates in square wave mode. The medium voltage switching frequency is at least three times that of the high voltage stage. In the particular simulation conditions the low voltage frequency is more than 15 times higher than that of high voltage stage. This number depends, however, on the magnitude control ratio.

The measured waveforms with same 80% reference amplitude are shown in figure 5. These measurements reflect, besides the quality superiority of the proposed inverter, that the inverter design meets its objectives regarding the switching frequencies at various stages.

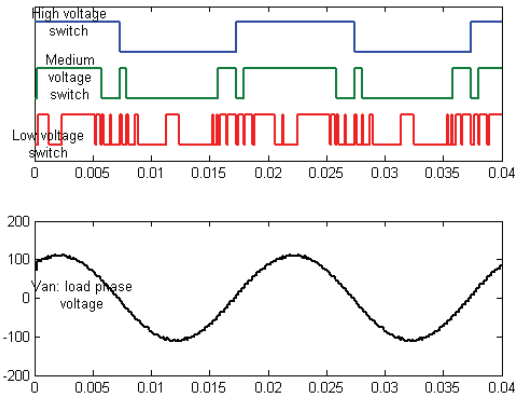
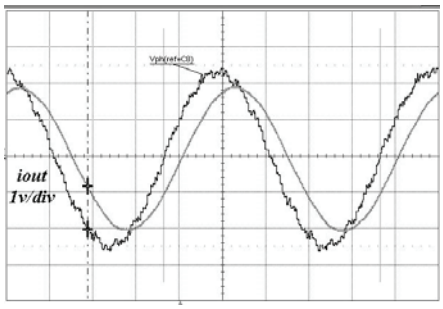
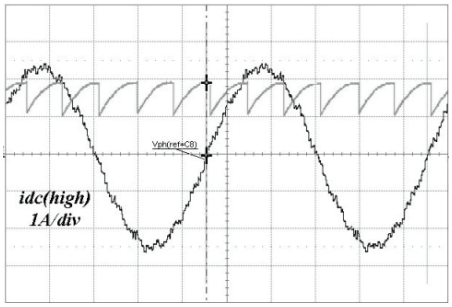


Fig. 4. Three stages switching signals and load phase voltage with 80% reference amplitude.



(a)



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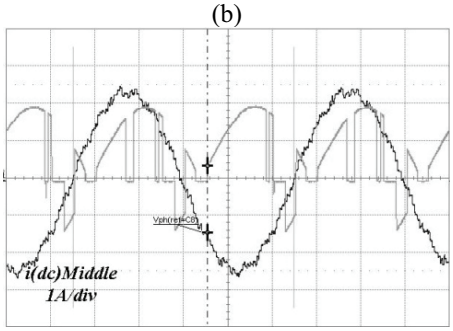

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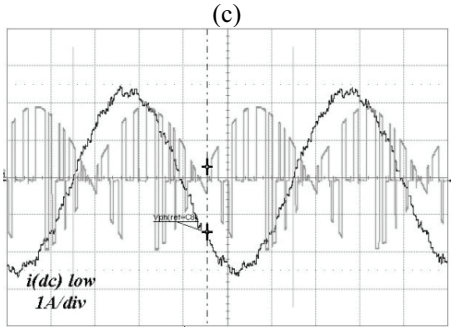

(d)

Fig. 5: Measurements with 80% reference supply load phase voltage with , a Load current, b. DC high voltage supply current, c. .DC medium voltage supply current, d. DC low voltage stage currents

6. CONCLUSION

In conclusion, we have presented a novel control strategy for the three-stage 18-level inverter. The described strategy exploits the inverters high resolution to approximate any reference vector by one of inverter vectors. The suggested strategy has been tested on low memory, fixed point processor DSP card and some details about this implementation have been given.

7. REFERENCES

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