DC Link Capacitor Voltage Balancing in Three Level Neutral point Clamped Inverter

Saad Mekhilef
Department of Electrical Engineering
University of Malaya
Kuala Lumpur, Malaysia
saad@um.edu.my

Hudhaifa Ibrahim Khudhur
Department of Electrical Engineering
University of Malaya
Kuala Lumpur, Malaysia
hudhaifaalzand@gmail.com

Hamza Belkamel
Department of Electrical Engineering
University of Malaya
Kuala Lumpur, Malaysia
hbelkamel@siswa.um.edu.my

Abstract—**Multilevel inverters are becoming increasingly popular for high and medium power applications. The diode clamped multilevel inverter (DCMLI) is an attractive high voltage multilevel inverter due to its robustness. The deviating voltage at the neutral point remains always a distracting feature in NPC inverter. For this reason DC link capacitors voltage balancing is crucial task in such configuration. The focus of this paper is a three-level three-phase neutral point clamped inverter. A modulation technique that balances the voltage in the DC link capacitors is presented. A Feedback voltage control method has been employed and a space vector pulse width modulation (SVPWM) is used as flexible technique to generate pulses that maintain a balanced DC link. The balancing is limited to an acceptable level without the use of the external active capacitor balancing circuit. To validate the effectiveness of the proposed method both simulation and experimental results are provided.**

Keywords-component; space vector modulation; diode clampedmultilevel inverter; feedback voltage control

I. INTRODUCTION

Most industrial processes aim to increase efficiency and reduce production costs. Given the existing power supply infrastructure for industries, these objectives can be achieved by increasing the size of power installations and increasing the power of all electrical machines involved. The required increase in power and efficiency can be approached in two ways: 1) by developing high-voltage semiconductors with voltage blocking capabilities of 3300, 4500, and 6500 V and 2) by developing a multilevel inverter.

For more than two decades, an immense attention has been paid to multilevel inverters due to their significant advantages power system. In Multilevel inverters construction, an array of power semiconductors, capacitors and DC voltage sources are used. Numerous multilevel converter topologies and wide variety of control methods have been developed in the recent literature. Three different basic multilevel converter topologies are commonly used which are the neutral point diode clamped (NPC); flying capacitor (FC) and the cascaded H-bridge (CHB) [1, 2].

The FC multilevel converter makes use flying capacitor for voltage clamping. To some extend these topologies are advantageous, Due to the transformer less operation and redundant phase leg states that make the semiconductor switches share the same distributed stress. The main drawback in such converters is the excessive number of storage capacitors for higher voltage steps. Because of its modularity and simplicity of control, The CHB configurations are better choice in high level applications. The distracting feature in this topology is the utilization of large number DC sources that makes the inverter complex and costly.

The NPC inverter topology (Fig. 2), introduced 25 years ago is the most widely used in all types of industrial applications [3], [4], usually operating in the range of 2.3 to 4.16 kV - with some applications up to 6 kV.

The main advantages of the three-level NPC voltage source inverter (VSI), over conventional two-level VSI for high-power applications are as follows.

- Voltage drop across the switches is half the DC bus voltage, effectively doubling the power rating of three level VSI's for a given power semiconductor device.
- The first voltage harmonics are centred at twice the switching frequency. This enables further reduction in size, weight, and cost of passive components while at the same time improving the quality of output waveforms.

The NPC inverter is widely used in more conventional high-power AC motor drive applications such as conveyors, pumps, fans, and mills, which offer power solutions for industries including oil and gas, metals, mining, marine, and chemical. The back-to-back configuration of this topology can also be used for regenerative applications such as in regenerative conveyors for the mining industry or grid interfacing of renewable energy sources like wind power. In most systems, three main methods (Fig. 1) are used to control the behaviour of the fundamental voltage generated by the three-level inverter to the load:1) selective harmonic elimination (SHE); 2) carrier-based pulse width modulation (CBPWM); and 3) space-vector modulation (SVPWM). All these modulation and control methods can be applied either to the motor side inverter or to the active front end (AFE) inputs [3-5].

978-1-4244- 9373-9/12/$26.00 ©2012 IEEE

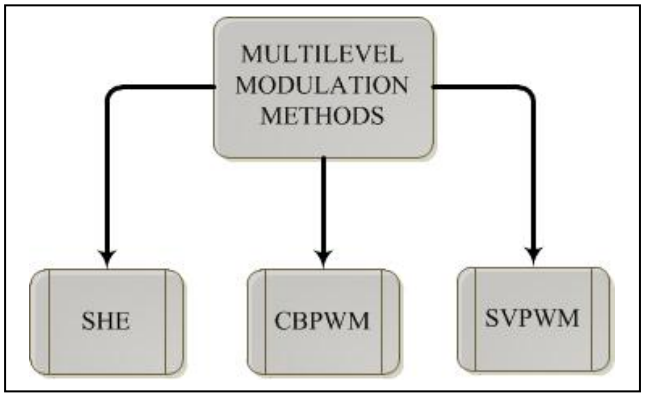

Figure 1 Modulation Methods for Three-level (NPC) Inverter.

Space-vector pulse width modulation (SVPWM) is one of the most advantageous of the modulation techniques as it offers significant flexibility to optimize switching waveforms, and because it is suited for implementation on a digital computer [5].

The main drawback of NPC topology is its unequal voltage sharing among series connected capacitors that result in dc-link capacitor unbalancing.

The neutral point, voltage balancing problem of three-level NPC VSI's has been widely addressed in literature resulting in various strategies being presented, and successful operation demonstrated with a DC-link voltage balance maintained. In addition, some of the proposed algorithms avoid narrow pulse problems, minimize losses by avoiding the switching of the highest internal current, or share the balancing task with active front end inverters [5-16].

Several methods were introduced for dc-link neutral point voltage balancing such as neutral point voltage balancing using equivalent states, neutral point voltage balancing using feedback voltage control, and neutral point voltage balancing using feedback dc current sign detection.

This paper studies the application of SVPWM control of a three-level NPC inverter in Simulink in order to investigate capacitor voltage balancing problem and to use the equivalent state to balance the DC capacitor voltage in the SVPWM controlled inverter.

II. Capacitor Voltage Balance for the NPC Inverter using the SVPWM

Figure 1 shows the power circuit of DCMLI. It is composed of two traditional two-level voltage source inverters stacked one over the other with some minor modification. Different methods have been proposed to control the DCMLI. SVPWM is one of the most advantageous of the modulation techniques as it offers significant flexibility to optimize switching waveforms, and its easy implementation on digital controllers.

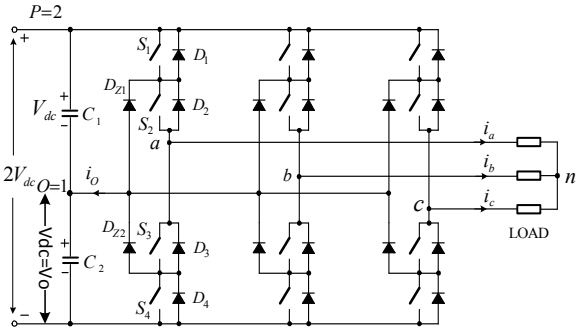

Figure 2 Three Phase Diode Clamped Multilevel Inverter

As mentioned earlier, the unbalanced voltage shared between the two series connected capacitors will affect the output voltage. To overcome this problem a control technique based on feedback voltage control is proposed.

The complete block diagram of the proposed SVPWM algorithm for three-level NPC inverter with an RL load is shown in Figure 3. The system contains essentially two sections. First, the power section shown in Figure 2 section (a) consists of the DC-link and the NPC inverter with R-L load. Second, the control section (modulator) as shown in Figure 2 section (b) consists of (1) coordinate transformation, (2) location of closest three vectors, (3) duty ratio calculation, (4) switching state selection and (5) switching sequence design.

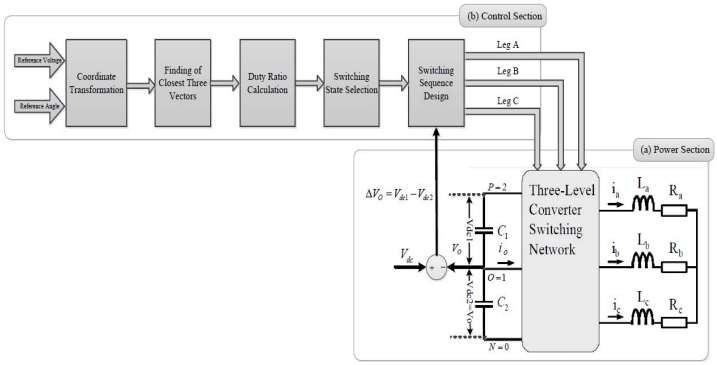

Figure 3 The Complete Block Diagram of SVPWM Algorithm for NPC Inverter

The main task of the modulator is to determine the position of the switches (switching state), and the switching duration (duty ratio) in order to synthesize the reference voltage vector. Thus, the modulator approximates the reference vector computed by the controller using the PWM of several switching vectors. Arguably, the best way to synthesize the voltage reference vector is by using the closest three vectors

III. EXPERIMENTAL SETUP AND RESULTS

Simulation of the proposed control algorithm for DCMLI was performed using MATLAB software. The design parameters used are 300 V as input voltage, two capacitor of 100 uF and 100Ω RL load with power factor between 1 to 0.5. to ensure the feasibility of the control algorithm, a prototype was manufactured. The proposed algorithm was implemented digitally in TMS320F28335 with Code Composer Studio. In the hardware implementation the DC input voltage was 200V . The obtained results are shown in Figures 4 to 7.

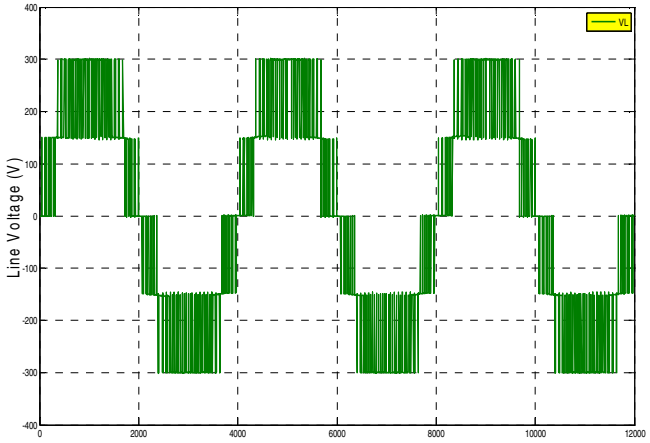

Figure 4: Simulated inverter line to line voltage

Figure 5: Experimental Dc link capacitors voltage

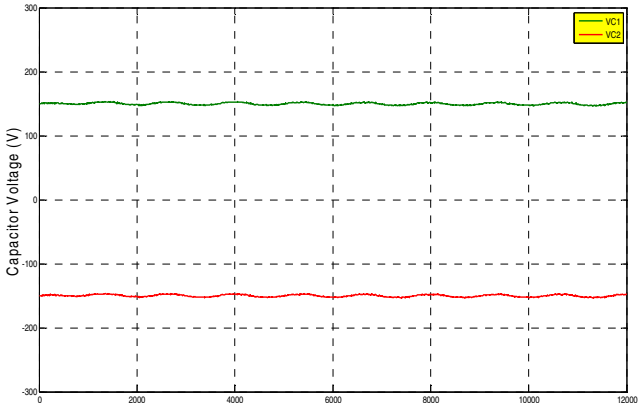

Figure 6 Simulated Dc link capacitors voltage

Figure 7 Experimental inverter line to line voltage

The results demonstrate that the proposed method can provide a level of neutral point voltage balancing, which is sufficient for most applications. Figures 6 and 7 show the consistent and almost equal voltage in both DC link capacitors. Such balance in the DC link makes the NPDC inverter drives a desired staircase waveform.

The presented modulation and voltage balancing techniques can be applied regardless of the number of the output levels.

IV. CONCLUSION

This paper discussed the SVPWM control technique. Such technique generally eased the DC-link unbalancing problem associated with these inverters. The SVPWM algorithm considered in this work is applicable to all inverters proving an output with any number of levels. The computational efficiency of this algorithm makes it a useful tool for further study of the characteristics of multilevel converters. More importantly, this technique provides flexibility in state selection that can reduce distortion and losses.

Acknowledgement

The authors would like to acknowledge the HIR-MOHE project. The research has been carried out under the Project no. UM.C/HIR/MOHE/ENG/ D000017- 16001

REFERENCES

[1] W. Chenchen and L. Yondong, "A survey on topologies of multilevel converters and study of two novel topologies," in *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*, 2009, pp. 860-865.

[2] J. Rodriguez, L. Jih-Sheng, and P. Fang Zheng, "Multilevel inverters: a survey of topologies, controls, and applications," *Industrial Electronics, IEEE Transactions on,* vol. 49, pp. 724-738, 2002.

[3] J. Rodriguez, S. Bernet, W. Bin, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *Industrial Electronics, IEEE Transactions on,* vol. 54, pp. 2930-2945, 2007.

[4] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *Industry Applications, IEEE Transactions on,* vol. 37, pp. 637-641, 2001.

[5] S. Mekhilef and M. N. Abdul Kadir, "Voltage Control of Three-Stage Hybrid Multilevel Inverter Using Vector Transformation," *Power Electronics, IEEE Transactions on,* vol. 25, pp. 2599-2606, 2010.

[6] S. Ogasawara and K. Akagi, "A vector control system using a neutral-point-clamped voltage source PWM inverter," in *Industry Applications Society Annual Meeting, 1991., Conference Record of the 1991 IEEE*, 1991, vol.1. pp. 422-427

[7] C. Newton and M. Sumner, "Neutral point control for multi-level inverters: theory, design and operational limitations," in *Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE*, 1997, pp. 1336-1343 vol.2.

[8] M. E. Ahmed,and S. Mekhilef, "Design and Implementation of a MultiLevel Three-Phase Inverter with Less Switches and Low OutputVoltage Distortion," Journal of Power Electronics, vol. 9, pp. 594-604,July 2009.

[9] S. Mekhilef,A. M. Omar, and N. A. Rahim, "Modeling of three-phase uniform symmetrical sampling digital PWMfor power converter," IEEE Transactions on IndustrialElectronics, vol. 54, pp .427-432, February 2007.

[10] S. Mekhilef, R. Saidur, and A.Safari, "A reviewon solar energy use in industries,"Renewable and Sustainable Energy Reviews, Elsevier, vol. 15, pp. 1777-1790,May 2011.

[11] M. N. A. Kadir,S. Mekhilef, and H. W. Ping, "Voltage Vector Control of a Hybrid Three-StageEighteen-Level Inverter by Vector Decomposition," IET Transaction onPower Electronics, vol. 3, pp. 601-611, July 2010.

[12] T. S. Ustun, and S.Mekhilef, "Effects of a Static Synchronous Series Compensator (SSSC)Based on Soft Switching 48-Pulse PWM Inverter on the Power Demand from theGrid," Journal of Power Electronics, vol. 10, pp. 85-90, January 2010.

[13] S. Mekhilef,and M. N. Abdul Kadir, "Novel Vector Control Method for Three-StageHybrid Cascaded Multilevel Inverter," IEEE Transactions on Industrial Electronics, vol. 58, pp. 1339-1349, April 2011.

[14] A. Safari, and S. Mekhilef, "Simulationand Hardware Implementation of Incremental Conductance MPPT with Direct ControlMethod Using Cuk Converter," IEEE Transactions on IndustrialElectronics, vol. 58, pp. 1154 -1161, April 2011.

[15] T. S. Ustun, and S. Mekhilef, " Designand Implementation of Static Synchronous Series Compensator with a soft-switching H-bridge Inverter with DSP-Based Synchronization Control,"International Review of Electrical Engineering (IREEE), vol. 5, pp. 1347-1353, July-August 2010.

[16] Mohamad N. Abdul Kadir, Saad Mekhilef "Dual Vector ControlStrategy for a Three-Stage Hybrid Cascaded Multilevel Inverter" Journal ofPower Electronics, vol. 10, no. 2, pp.155-164, 2010