Design A Stable 14-To-20-GHz Source

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Abstract: Careful selection of key components and the use of straightforward multiplication schemes can be applied to the design of a low-noise frequency synthesizer for Ku-band signals to 20 GHz.

Frequency synthesizers provide the local oscillator (LO) signals as well as transmit signals in many communications networks. They must be stable, with low phase noise and good spectral purity, to support the complex modulation formats that are now common to many wired and wireless communications networks. To serve as a signal source in such networks, a low-noise frequency synthesizer capable of tuning from 14 to 20 GHz (Ku-band operation) was developed with step size of 500 kHz and phase noise of -81 dBc/Hz offset 10 kHz from the carrier. By doubling the output of this 20-GHz frequency synthesizer a total of three times, it can be extended in frequency for millimeter- wave radar systems and radio links operating at frequency bands of 57 to 64 GHz and 71 to 77 GHz. Improvements in silicon CMOS technology, notably its enhanced capabilities for RF, microwave, and even millimeter-wave circuits, have supported its expanding applications in wireless transmission applications. Silicon CMOS, for example, is suitable for fabricating both highfrequency oscillators as well as integrated frequency synthesizers. As a result of device geometry scaling, CMOS transistors have been developed with transition frequencies well into the millimeter-wave range. Practical CMOS wireless source solutions require a choice of the optimal frequency synthesizer architecture to meet the different requirements of a given application.

For example, integer-N frequency synthesizers can be challenged when meeting different performance specifications, such as loop bandwidth, low phase noise, and narrow channel spacing, due to the integer-N divider modulus and its fundamental design limitations. Fractional-N frequency synthesizers can provide the desired loop bandwidth with small channel spacing without suffering from high phase noise and reference spurious content. Since they use higher phase/frequency-detector (PFD) comparison frequencies and lower divider ratios compared to integer-N frequency synthesizers, fractional-N frequency synthesizers can achieve reasonably good lowfrequency phase noise.[1-3]

Frequency synthesizers can be categorized into direct and indirect frequency synthesizer types.[4]

In a direct frequency synthesizer, there is no feedback loop to lock the reference clock with the feedback clock. Direct frequency synthesizers can be further categorized as direct analog synthesizers (DASs) and direct-digital synthesizers (DDSs). Indirect frequency synthesizers

can be classified as delay-lockloop (DLL)-based and phase-lock-loop (PLL)-based synthesizers.[5]

In a DAS, a frequency mixer is fed by a voltage-controlled oscillator (VCO) and an external source to generate additional frequency components. When the loop in this type of synthesizer operates under locked conditions, the signal frequencies entering the PFD are exactly the same. The problem with this method is the possibility of two mixed products being able to give the correct phase or frequency comparison as shown in ***Fig. 1***.[6,7]

In the DDS shown in ***Fig. 2***, the output frequency is directly proportional to the input frequency. On the other hand, in the indirect frequency synthesizer of ***Fig. 3***, the divide-by-N feedback output is compared with a reference frequency, generating a comparison frequency. The comparison frequency is integrated by loop filter and steers the VCO frequency to minimize the comparison frequency. Filtering is an essential stage of the process to eliminate harmonics and other unwanted spurious frequencies related to the initial frequency components.[8] The PFD, divide-by-N divider, and loop filter are usually fabricated together within an integrated circuit (IC). Some commercial ICs may also include a VCO integrated with a dual-modulus prescaler or other divider circuitry. Although in some circuits all the components can be defined, such as the N integer in a divide-by-N divider.[9-15]

In an indirect frequency synthesizer, the VCO's frequency range is limited to present the loop from operating in an unstable or undesirable state. This condition limits the total bandwidth of the design (***Fig. 4***). On the other hand, in DDS structure a programmable divider or counter is provided to generate fractions of VCO frequency for phase or frequency comparison in PFD as shown in ***Fig. 5***.

The block diagram of a proposed fractional-N synthesizer frequency is illustrated in ***Fig. 6***. It consists of a reference frequency source, phase/ frequency detector with charge pump (PFD-CP), loop filter, voltage-controlled oscillator (VCO), and division modulus. The division modulus can work with fractional division values that leads to fractional adjacent frequencies set by the reference frequency, f_{ref}. The channel spacing is set by these fractional frequencies ($0.1 \times f_{ref}$). The fractional N structure can enter a "locked" or stabilized state much faster than an integer-N frequency synthesizer structure since the reference frequency is no longer restricted in terms of phase noise and loop bandwidth.[9]

The division ratio is given by:

$$N_{average} = N_{int} + N_{fractional} \quad (1)$$

A k-bit accumulator is used to interpolate between the two integers (A and B). D is a k-bit word representing the decimal part of factor $N_{average}$. The accumulator generates a carry-out bit every D times of 2k cycles of the PFDCP comparison frequency. Thus, if the carry-out bit is used to toggle between Nint and Nint + 1, the divider will divide by D (N_{int} + 1) times and by N_{int} (2k – D) times over a 2^k cycles interval, so that:

$$N_{average} = [D(N_{integer} + 1) + (2^k - D) N_{integer}]/2k = N_{integer} + D/2^k \quad (2)$$

In PLL-based frequency synthesizers, the loop filter must suppress the high-frequency components of the charge pump output current.[3] Second- or third-order loop filters are

commonly used for charge-pumped frequency synthesizers with an external loop filter. However, these types of loop filters cannot be fabricated as part of a monolithic frequency synthesizer IC; for a loop bandwidth of a few kilohertz, the total capacitance of the required loop filter can be as large as a few nanoFarads, which is too large a capacitor for fabrication as part of an IC semiconductor process.

A 14-to-20-GHz frequency synthesizer can be designed by means of one VCO and the appropriate divider circuitry to achieve the 14-to-20-GHz frequency range.[10-13] It can also be accomplished by designing a frequency synthesizer to operate within a lower frequency-band allocation[14,15] and then multiplying the output of that frequency synthesizer to reach the required 14-to-20-GHz range. Because of the paucity of VCOs with low phase noise in the required frequency band, the second method was chosen as the desired design strategy. The approach started by selecting a VCO with low phase noise in the 1.8-to-2- .4-GHz frequency range to assemble a frequency synthesizer that operates from 1.8 to 2.4 GHz. By multiplying the output of that frequency synthesizer, low-noise signals from 14 to 20 GHz can be achieved (***Fig. 6***).

The design began by selecting a voltage-controlled oscillator (VCO) with low phase noise, a model ROS- 2432-119+ VCO IC from Mini-Circuits. This compact VCO tunes from 1662 to 2432 MHz with +5.5 dBm nominal output power and typical phase noise of -100 dBc/Hz offset 10 kHz from the carrier and -122 dBc/Hz offset 100 kHz from the carrier. The VCO is supplied in a surface-mount package measuring 0.5 x 0.5 in.

In addition, a model ADF4118 3-GHz PLL frequency synthesizer IC from Analog Devices was selected to stabilize the output frequency of the VCO. The ADF4118 consists of a low-noise digital PFD, precision charge pump, programmable reference divider, programmable A (5-b) and B (13-b) counters, and a dual-modulus prescaler. A 14-b reference counter provides flexibility when selecting reference frequencies at the input of the PFD. The ADF4118 is designed to form a complete PLL synthesizer by adding a VCO and external loop filter and can be controlled by a simple three-wire interface.

As the reference oscillator, a model TXO200U temperature-compensated crystal oscillator (TCXO) from Rakon Ltd. was selected. The 10-MHz fixed-frequency oscillator exhibits phase noise of -150 dBc/Hz offset 10 kHz from the carrier. These key components were assembled into the Ku-band frequency synthesizer represented schematically in ***Fig. 9***. ***Table 1*** shows the results of phase-noise measurements from 1.8 to 2.4 GHz at offset frequencies of 1 kHz, 10 kHz, 100 kHz, and 1 MHz. To reach the final frequency range of 14 to 20 GHz, the frequency synthesizer employs a three-step multiplication scheme (***Figs. 7*** and ***8***). The circuit of ***Fig. 9*** was used in a computeraided- engineering (CAE) simulation of the synthesizer, with measured performance shown in ***Fig. 10***. ***Table 2*** shows the results of phase-noise measurements at various carrier and offset frequencies.

As was shown, a low-noise millimeter- wave source can be fabricated in several steps starting from a relatively low-frequency oscillator, provided that the starting point is capable of good low-phase-noise performance. The first step involved designing a low-noise frequency synthesizer capable of output frequencies from 1.8 to 2.4 GHz. Then, by multiplying the output frequency by integer 8, it was possible to translate these frequencies to a range of 14 to 20 GHz. As a result of the multiplication, the phase noise is reduced by a factor of 20log8, although this is still acceptable for many communications applications. By further

multiplication, using a factor of 4 multiplication, output frequencies from 57 to 77 GHz can be produced for use in millimeterwave radar systems and point-to-point radios.

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