SHEPWM Based New Hybrid Multilevel Inverter Topology with Reduced Switch Count

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Keywords

«Multilevel Converters», «Pulse Width Modulation (PWM)», «Power Semiconductor Devices» «Power Conditioning»

Abstract

In this paper, a new single-phase hybrid multilevel inverter topology is proposed with reduced switch count. The basic unit of the proposed topology is capable of generating 13 levels at the output. A higher number of levels can be generated by extending the basic unit. Two different extensions of the basic unit have been proposed in the paper. The topology consists of a level generation unit (LGU) and the polarity changing unit (PCU). The level generation unit of the proposed topology is based on the series connection of multiple switched dc voltage sources with half and full bridge configurations. Selective Harmonic Elimination PWM (SHEPWM) based switching control technique has been employed for an improved harmonic spectrum. Performance and effectiveness of the proposed topology with the employed SHEPWM control have been substantiated by simulation results and verified by experimental results obtained from a laboratory prototype.

Introduction

With the technological advancements and the added advantages over conventional two-level inverters, the multilevel inverters have allowed increased focus owing to their evolving topologies. MLIs offer reduced voltage source counts, decreased switches and driver circuits in addition to high power quality, low harmonic distortion and reduced switching losses. With the advantage of a wide range of applications, they are used in the variable frequency drives, HVDC and Flexible AC transmission structure, Electric Vehicle drive, renewable energy systems, etc. The very first mentioned MLIs in literature are cascaded H-bridge MLI, Flying Capacitor MLI, and Diode Clamped MLI [1]–[4]. Numerous topologies have been presented in the literature with the aim of achieving a higher level of output voltage with reduced switch counts [5]–[8]. To increase the number of voltage levels with reduced switch counts, several MLIs have been demonstrated in [7], [9]–[13].

A new MLI topology has been proposed in [14], which uses 12 switches for the nine-level voltage generation. A similar topology has been proposed in [10], which uses three dc voltage source with seven switches for nine level output voltage. However, with four diodes used in the topology, the efficiency of the topology [10] has a poor value. The topologies proposed in [15] gives the optimal design of the topology, however, the required number of dc voltage sources are on the higher side. This paper proposes a new MLI topology with reduced switch and source count. The basic unit of the proposed topology uses 10 switches with three dc voltage sources to produce the 13 level output voltage waveform. The paper is organized as follows: Section II gives the details of the basic unit with the two extention of basic unit. Section III deals with the comparative study of the proposed basic unit. Section IV gives the details of the SHEPWM used for the optimal switching angle calculations. Section V provides the simulation hand hardware results and the paper is summarized in Section VI.

Proposed Topology

The basic unit of the proposed multilevel inverter is depicted in Fig. 1. The proposed topology consist of two units i.e. level generation unit (LGU) and polarity change unit (PCU). LGU consist of three dc voltage sources along with six unidirectional switches S_1-S_6. The switch pair (S_1-S_2), (S_3-S_4), and (S_5-S_6) need to be operated in complementary mode to avoid short-circuiting of dc voltage sources. With $V_1=3V_{dc}$, $V_2=2V_{dc}$, and $V_3=V_{dc}$, the LGU generates six levels in positive polarity. The PCU is an H-bridge, which consist of four unidirectional switches (H_1-H_4). The PCU is used to change the polarity with the generation of zero voltage level at the output. Therefore, the combination of these two units generates 13 levels of the output voltage across the load. Table I gives all the switching states of the proposed basic unit.

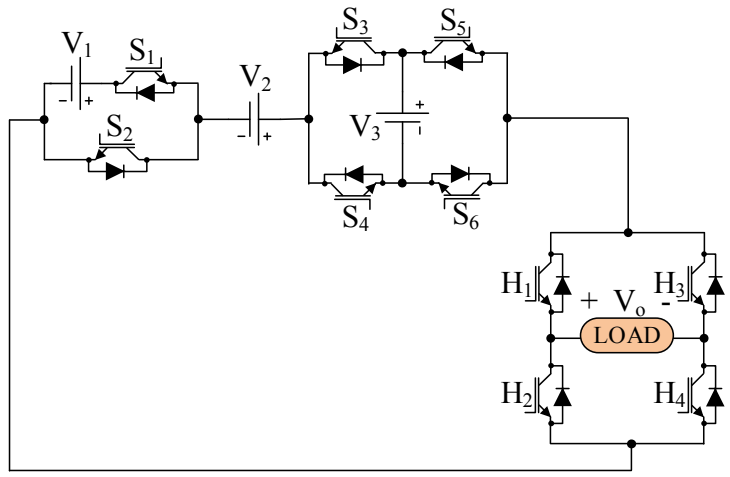


Fig. 1: Proposed MLI topology

Table I: switching states of proposed basic unit with $V_1=3V_{dc}$, $V_2=2V_{dc}$, and $V_3=V_{dc}$

Switches of LGU						Switches of PCU				V_o
S_1	S_2	S_3	S_4	S_5	S_6	H_1	H_2	H_3	H_4	
0	0	0	0	0	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0	1	V_{dc}
0	1	1	0	1	0	1	0	0	1	$2V_{dc}$
0	1	0	1	1	0	1	0	0	1	$3V_{dc}$
1	0	1	0	0	1	1	0	0	1	$4V_{dc}$
1	0	1	0	1	0	1	0	0	1	$5V_{dc}$
1	0	0	1	1	0	1	0	0	1	$6V_{dc}$
0	0	0	0	0	0	0	1	0	1	0
0	1	1	0	0	1	0	1	1	0	$-V_{dc}$
0	1	1	0	1	0	0	1	1	0	$-2V_{dc}$
0	1	0	1	1	0	0	1	1	0	$-3V_{dc}$
1	0	1	0	0	1	0	1	1	0	$-4V_{dc}$
1	0	1	0	1	0	0	1	1	0	$-5V_{dc}$
1	0	0	1	1	0	0	1	1	0	$-6V_{dc}$

For a higher number of levels at the output, the basic unit of the proposed topology can be extended with three different connections as explained below.

A. 1st Extension: In the 1st extension, the dc voltage source configured as a half-bridge on the left side of the voltage source V_2 of the basic unit are added. This extension is shown in Fig. 2. The different equations for the 1st extension with *m* numbers of dc voltage sources configured in half bridge are given as:

$$\left.\begin{aligned} N_{sw} &= 2m + 8 \\ N_{dc} &= m + 2 \\ N_L &= 3 \times 2^{m+1} + 1 \end{aligned}\right\} \quad (1)$$

The magnitude of dc voltage source V_{Lm} is selected as given in (2).

$$V_{Lm} = 3 \times 2^m \quad (2)$$

B. 2nd Extension: In this extension as depicted in Fig. 3, full bridge configured dc voltage sources are added on the right side of the voltage source V_2 of the basic unit. The magnitude of dc voltage sources of the full bridge is selected in tertiary mode. Therefore, the voltage magnitude of V_{L1} is selected based on the number of full bridge configured dc voltage sources. The different equations for 2nd extension with *n* number of dc voltage sources on the right side of voltage source V_2 are given as:

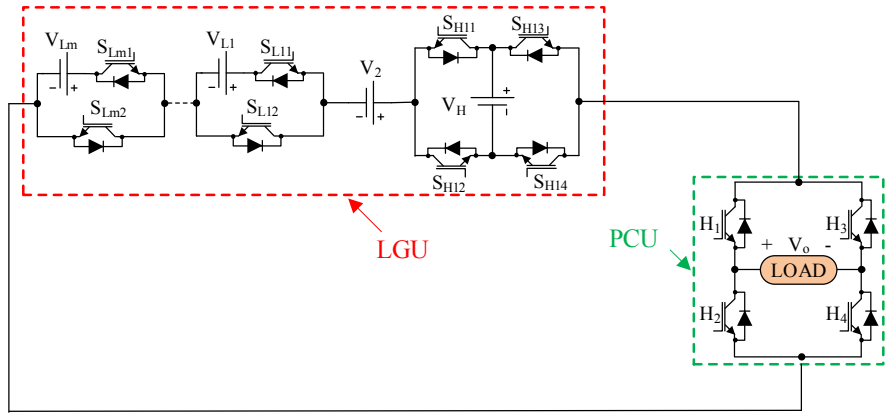


Fig. 2: Extension of basic unit with addition of dc voltage sources configured in half bridge

$$\left.\begin{aligned} N_{sw} &= 4n + 6 \\ N_{dc} &= m + 2 \\ N_L &= 3(3^n + 1) + 1 \end{aligned}\right\} \quad (3)$$

The magnitude of dc voltage sources are selected as:

$$\left.\begin{aligned} V_{L1} &= 3^n \\ V_{Hn} &= 3^{n-1} \end{aligned}\right\} \quad (4)$$

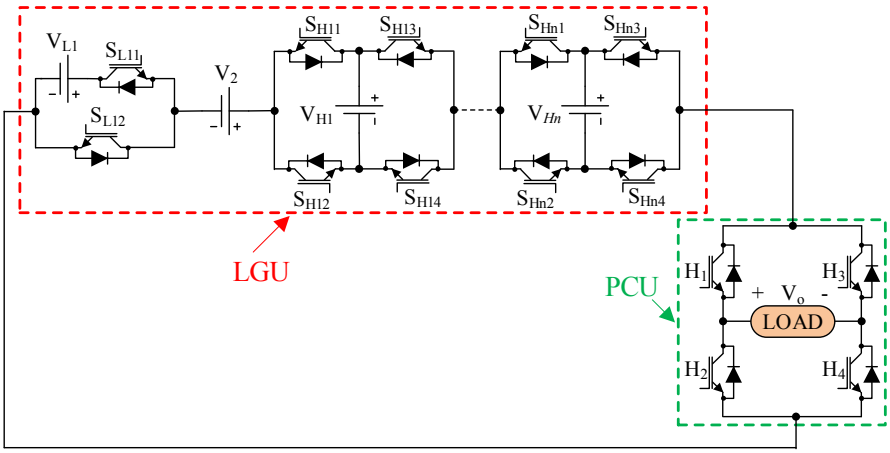


Fig. 3: Extension of basic unit with addition of dc voltage sources configured in full bridge

Comparative Study

Table II compares the different multilevel inverter topologies with three dc voltage sources in terms of the number of total semiconductor devices against a number of levels. The topology introduced in [15] uses a lower number of power semiconductor devices compared to other topologies but generated 11 levels at the output. The basic unit of the proposed topology generates the maximum number of levels compare to other topologies.

Table II: Comparison of different multilevel inverter topologies with **Three Voltage Sources**

Topology	Number of Switches	Number of Diodes	Total Semiconductor Devices	Number of Levels
[11]	7	4	11	9
[10]	7	4	11	7
[12]	8	0	8	7
[15]	8	0	8	11
Proposed	**10**	**0**	**10**	**13**

Selective Harmonic Elimination (SHE) Modulation Technique

Fig. 4 shows the staircase output voltage waveform. For a high-quality output voltage, the total harmonic distortion (THD) is an important factor and is given by

$$THD = \frac{\sqrt{\sum_{i=2}^{n}(V_i)^2}}{V_1} \quad (5)$$

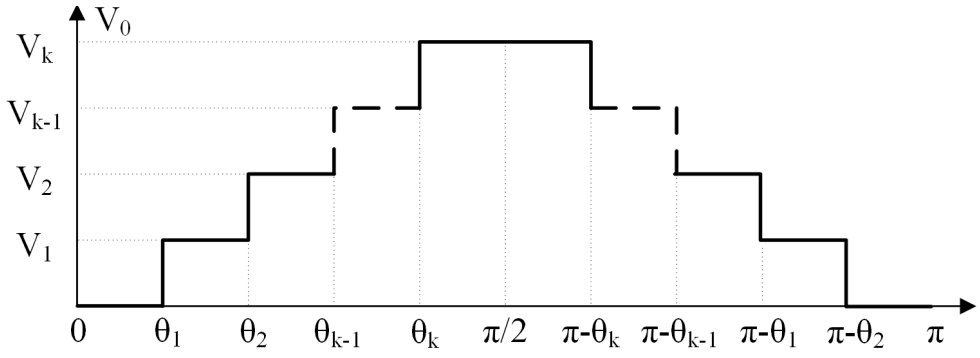


Fig. 4: Staircase output voltage

Where V_1 is the fundamental component of the output voltage and V_i is the i^{th} harmonic voltage. Selective harmonic elimination (SHE) modulation technique demonstration superior performance due to its capability of eliminating lower order harmonics [16]. For 13 level output voltage, five harmonic voltages can be eliminated. In this paper 3rd, 5th, 7th, 9th and 11th harmonic order is selected to be eliminated. The equations for 13 level SHEPWM is given as

$$b_1 = \frac{4V_{dc}}{\pi}[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) + \cos(\theta_6)] = V_D \quad (6)$$

$$b_3 = \frac{4V_{dc}}{3\pi}[\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) + \cos(3\theta_4) + \cos(3\theta_5) + \cos(3\theta_6)] = 0 \quad (7)$$

$$b_5 = \frac{4V_{dc}}{5\pi}[\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) + \cos(5\theta_6)] = 0 \quad (8)$$

$$b_7 = \frac{4V_{dc}}{7\pi}[\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) + \cos(7\theta_6)] = 0 \quad (9)$$

$$b_9 = \frac{4V_{dc}}{7\pi}[\cos(9\theta_1) + \cos(9\theta_2) + \cos(9\theta_3) + \cos(9\theta_4) + \cos(9\theta_5) + \cos(9\theta_6)] = 0 \quad (10)$$

$$b_{11} = \frac{4V_{dc}}{3\pi}[\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) + \cos(11\theta_6)) = 0 \quad (11)$$

Where $b_1 = V_D$ is the fundamental component of the output voltage and gives the desire output voltage V_D. $b_3, b_5, b_7, b_9,$ and b_{11} are the harmonic orders to be eliminated and made equal to zero. The modulation index m_a is given by

$$m_a = \frac{\pi \times V_D}{4 \times N \times V_{dc}} \quad (12)$$

The switching angles $\theta_1 - \theta_6$ are obtained from the solution of (6)-(12). The variation of these angles are shown in Fig. 5 (a) and Fig. 5 (b) shows the variation of harmonic orders against the modulation index m_a.

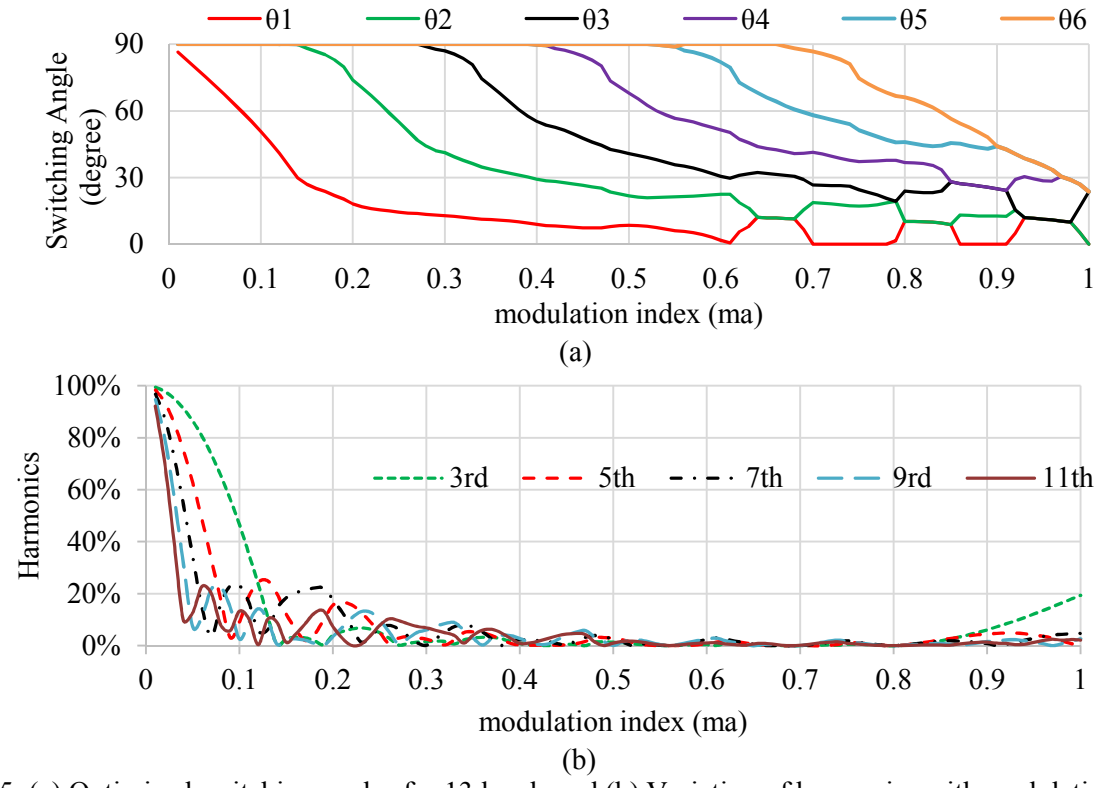


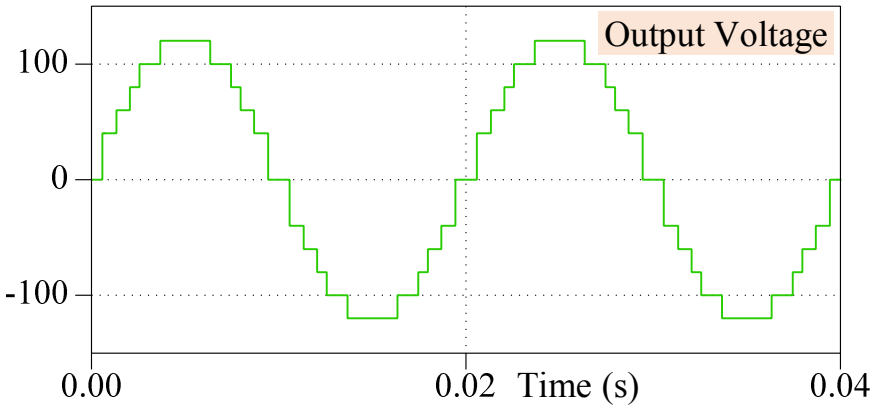
Fig. 5: (a) Optimized switching angles for 13 levels and (b) Variation of harmonics with modulation index for 13 level

Table III: Optimized switching angles (Degree)

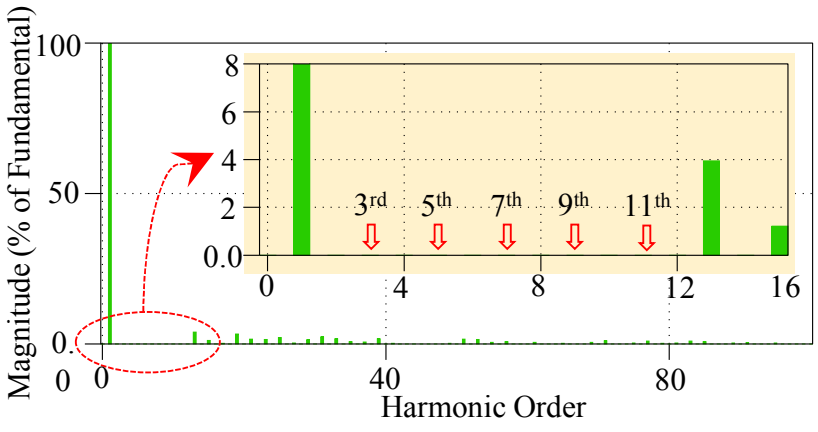
m_a	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6
0.8	10.20	10.20	23.87	36.70	46.00	66.10

Results and Discussion

The MATLAB/Simulink software is used for the validation of the proposed topology in different loading conditions. All the simulation results provided in this section are carried out at modulation index of 0.8. The switching angles calculated by SHEPWM at the m_a=0.80 is given in Table III. Fig. 6 (a) shows the output voltage waveform using the switching angels calculated by SHEPWM. Fig. 6 (b) displays the FFT of the output voltage. From the FFT, the 3rd, 5th, 7th, 9th and 11th harmonic are zero as selected in SHEPWM. After fundamental, 13th harmonic is present in the output voltage with magnitude less than 4%. The elimination of selected harmonics order shows the effectiveness of SHEPWM.

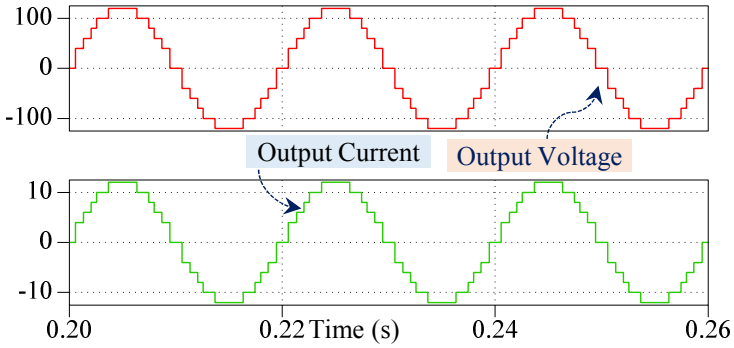


(a)

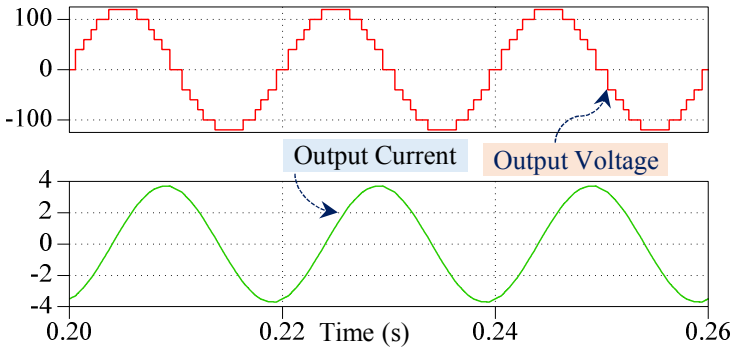


(b)

Fig. 6: Output voltage waveform (a) and FFT of output voltage with SHEPWM (b) at modulation index of 0.8



(a)



(b)

Fig. 7: Output voltage and current waveform with (a) Z = 10Ω and (b) Z = 10Ω+100mH

Furthermore, the proposed topology has been tested with differet types of load. The output voltage and current waveform with a purely resitive load having a magnitude of 10Ω is shown in Fig. 7 (a). Similarly, the output voltage and current waveforms with a series connected resistive-inductive load with Z = 10Ω+100mH has been depicted in Fig. 7 (b).

Based on the analyses and simulation of the proposed topology, an experimental prototype of the proposed topology is built as illustrated in Fig. 8. TOSHIBA IGBT GT50J325 is employed as a switch in the prototype. The gate pulses for the switches are produced by

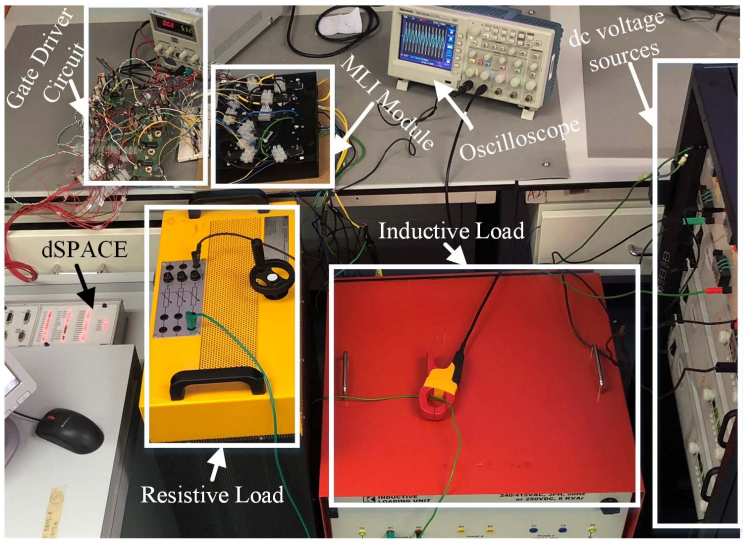


Fig. 8: Hardware setup

means of dSPACE CP1104 with SHEPWM. The isolated dc voltage source magnitude is selected as V_1=30V, V_2=20V, and V_3=10V. The peak of the output voltage is 60V with voltage step of 10V. The experimental output voltage and its FFT for 13-level output voltage with a modulation index of 0.8 are demonstrated in Figs. 9 (a) and (b). Additionally, the performance of suggested topology is also studied for resistive and series connected resistive-inductive load. The values used for the load parameters are as R=20Ω and L=100mH. Figs. 9 (c) and (d) shows the output voltage and current for R load and RL load respectively.

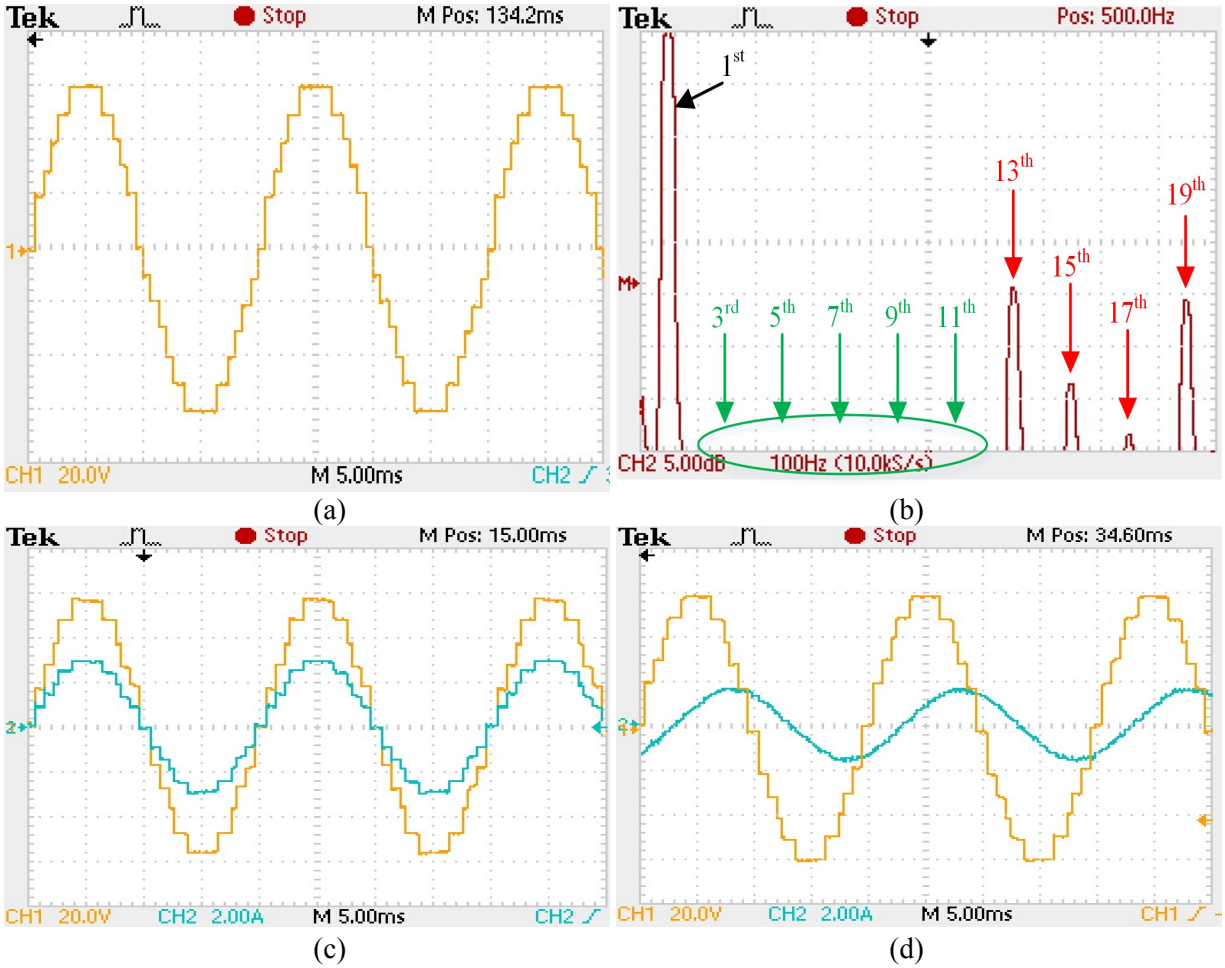


Fig. 9: Experimental results of (a) Output voltage, (b) FFT of output voltage, (c) output voltage and current with R load and (d) Output voltage and current with RL load

Conclusion

This paper has demonstrated a new hybrid multilevel inverter with reduced counts of semiconductor devices. The proposed topology is able to generate 13-level output voltage using ten switches. Selective harmonic elimination PWM method is used for the elimination of lower order harmonics of the output voltage which is thereby verified through simulation and experimental results. The performance validation of the synthesized inverter is achieved with different types of load.

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