# A Highly Efficient Single-phase Transformerless H-bridge Inverter for Reducing Leakage Ground Current in Photovoltaic Grid-connected System

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**Abstract**—In this article, the performance of the split-capacitor H-bridge topology as a single-phase transformerless photovoltaic inverter is studied. By connecting the midpoint of its two series DC-link capacitors to the ground, the split-capacitor H-bridge is able to clamp the common-mode voltage of the system, effectively suppressing leakage ground current. To overcome the issue of capacitor voltage balancing, a simple balancing circuit and its control are introduced. The operation modes, common-mode voltage, and leakage ground current characteristics of the split-capacitor H-bridge topology are discussed, subsequently validated using both simulation and experimental tests. Comparison with a conventional transformerless H-bridge topology proves the superiority of the split-capacitor H-bridge topology in terms of leakage ground current and efficiency.

## 1. INTRODUCTION

Solar PV is a popular renewable energy source that has contributed to the total energy consumed in the world. In most regions, with the help of governmental incentives and rising awareness, their usage becomes more and more widespread. Most existing PV grid-connected inverter systems incorporate a line transformer or high-frequency transformer in the systems to provide isolation between the utility grid and the PV module so that issues on electrical safety hazard can be avoided [1]. This gain in electrical safety comes with a price of increased system size and cost, as transformers are known to be bulky and costly.

To achieve higher efficiency, lower cost, lighter weight, and smaller size, various transformerless PV grid-connected inverter topologies have been proposed [2–7]. The current practice requires the PV module frame to be connected to the ground to comply with safety regulation and standards. Figure 1 shows the PV system installation without an isolation

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## NOMENCLATURE

| | | | | | |
|---|---|---|---|---|---|
| AC | = | alternating current | $L_{f1}$ | = | filter inductor at line inverter side |
| $C_{pv}$ | = | photovoltaic parasitic capacitance | $L_{f1n}$ | = | filter inductor at neutral inverter side |
| $C_{pv}$ | = | photovoltaic parasitic capacitance | $L_b$ | = | balancing circuit inductance |
| $C_{B1}, C_{B2}$ | = | DC-link capacitor | NPC | = | neutral point capacitor |
| $C_f$ | = | filter capacitor | PV | = | photovoltaic |
| DC | = | direct current | PWM | = | pulse-width modulation |
| DSP | = | digital signal processor | $Q_1$–$Q_4$ | = | H-bridge inverter switches |
| EMI | = | electromagnetic interference | $Q_{B1}, Q_{B2}$ | = | balancing circuit switches |
| FFT | = | fast Fourier transform | SC-HB | = | split-capacitor H-bridge |
| HB-ZVR | = | H-bridge zero voltage rectifier | SPWM | = | sinusoidal pulse-width modulation |
| HERIC | = | high-efficiency reliable inverter concept | THD | = | total harmonics distortion |
| $I_g$ | = | leakage ground current | $V_{PV}$ | = | DC voltage |
| $L_{f2}$ | = | filter inductor at line grid side | $V_g$ | = | ground voltage |
| $L_{f2n}$ | = | filter inductor at neutral grid side | $\Delta_{ripple,max}$ | = | maximum ripple |

transformer. As seen in the figure, parasitic capacitance ($C_{pv}$) appears between the output terminals of the PV module (positive and negative output PV terminals) and the ground, forming a low impedance path for leakage current to flow. The value of this parasitic capacitance varies with various factors, such as the surface area of the PV module and grounded frame, the distance of PV cell to the module, and the atmospheric conditions [8]. Nevertheless, this parasitic capacitance takes a value between 50–150 nF/kW [9–11].

Due to the presence of parasitic capacitance between the PV module and system ground, significant leakage ground current can flow in the transformerless PV inverter systems [1, 9, 12, 13]. With reference to German standard VDE0126–1–1, the amplitude of leakage ground current must be less than 300 mA RMS to avoid an electrical hazard when the PV array is touched [9]. Apart from safety concerns, leakage ground current also causes increased grid current harmonics and reduces the efficiency of the whole system [12, 13]. In [2–7, 14], it was shown that the leakage ground current is caused by the fluctuating common-mode voltage. Hence, to reduce leakage ground current, the common-mode voltage should be constant. Furthermore, the fluctuation of common-mode voltages will increase the voltage stress d$v$/d$t$ of devices and reduce the lifetime of device as well [13, 14].

Leakage ground current through the parasitic capacitance of the PV module can be reduced in several ways subject to the converter topology, switching strategy, and AC filter [8, 11]. In terms of switching strategy, the commonly used unipolar SPWM is not suitable for a transformerless system due to the fact that this PWM method generates varying common-mode voltages [8, 11]. To reduce the leakage ground current in the H-bridge inverter, the use of a bipolar SPWM tech-



**FIGURE 1.** Transformerless PV system installation.

nique was proposed in [11]. However, for the same switching frequency, this switching technique gives twice the grid current ripple and higher THD compared to the unipolar SPWM technique [11].
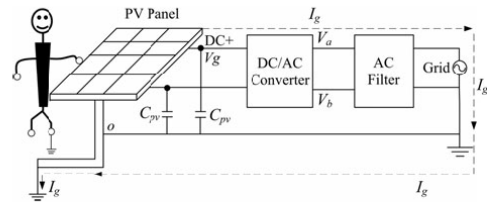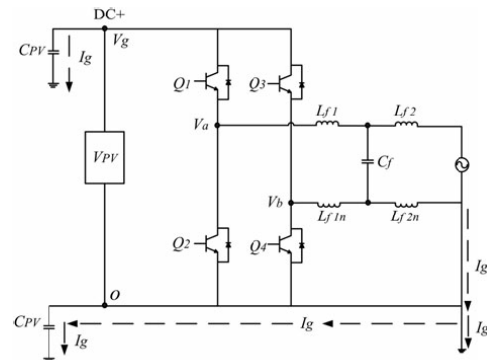


**FIGURE 2.** Transformerless inverter using conventional H-bridge topology.
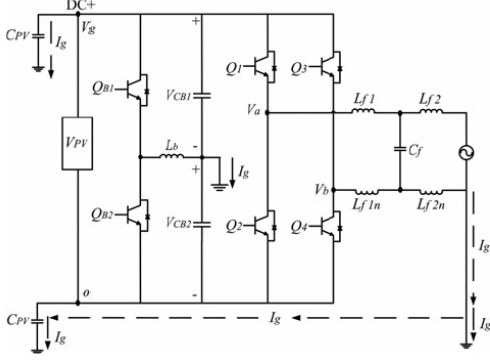
**FIGURE 3.** SC-HB transformerless inverter topology.

Recently, some new transformerless single-phase H-bridge inverters with unipolar SPWM were presented [2–7, 15–18]. By disconnecting the PV array from the grid during zero vector state, low leakage ground current can still be attained in these topologies even with the use of unipolar SPWM. The disconnection can be done either by an AC bypass or a DC bypass. The AC-bypass is provided using an additional switch on the inverter AC side between the inverter and the grid, whereas the DC bypass uses an additional switch on the inverter DC side between the H-bridge inverter and PV array. The AC bypass was proposed in HB-ZVR [2, 3] and HERIC topologies [4]. On the other hand, the DC bypass was introduced in H6, H5, and oH5 topologies [5–7]. Apart from the AC and DC bypass methods, another solution for reducing current leakage is connecting the mid-point of the DC-link capacitor to the neutral line of the grid, as in an NPC topology [16, 17]. However, this topology requires a high-voltage DC link up to 700 V.

The leakage ground current ($I_g$) through the parasitic capacitance ($C_{pv}$) can be analyzed with the common-mode voltage ($V_{cm}$) at an output inverter terminal point, as shown in Figure 1. The common-mode voltage is defined as the average sum of both output inverter ($V_{ao}$ and $V_{bo}$) and the common reference. The common reference is taken from the negative terminal of the PV module marked with 0. The estimation value of common-mode voltage ($V_{cm}$), which is imposed by the PWM inverter, is expressed by

$$V_{cm} = \frac{V_{ao} + V_{bo}}{2}. \tag{1}$$

To avoid leakage ground current flow through parasitic capacitance ($C_{pv}$), the common-mode voltage must be kept constant during all commutation states of the inverter switching technique, as proposed in [2–7]. In [2], it was shown that instead of measuring $V_{ao}$ and $V_{bo}$ then calculating $V_{cm}$ from Eq. (1), the impact of $V_{cm}$ can also be evaluated by measuring the

voltage between the DC+ and the system ground (denoted as $V_g$, as seen in Figure 1), which is a simpler measurement in the experimental setup.

Figure 2 shows a conventional H-bridge topology commonly used as a single-phase inverter. Even though it is simple, this topology is not well suited as a transformerless PV inverter due to the possible flow of high leakage current. Other transformerless topologies, such as those in [2–7], requires additional switches and diodes, which increases the overall system cost. Here, a simple alternative single-phase transformerless topology that is capable of suppressing leakage ground current ($I_g$) is studied. This topology, recognized as the SC-HB inverter, has a grounded connection at the mid-point of its two series DC-link capacitor, as shown in Figure 3. As a result of this connection, an almost constant commn-mode voltage can be attained. Hence, the leakage ground current can be significantly suppressed.

Due to the use of a series-connected capacitor, the issue of capacitor voltage balancing needs to be considered for the SC-HB topology. To mitigate this problem, a balancing circuit employing auxiliary DC-DC converter [18–20] is adopted here. The details of this approach are further explained in Section 3. The performance of the whole system is validated using both simulation and experimental tests and compared with conventional H-bridge topology. The results show that the SC-HB topology is simple yet able to keep the leakage ground current well below the international standard requirement. At the same time, it is found that the SC-HB topology provides high efficiency throughout the whole power range compared to conventional H-bridge topology, making it a promising candidate as single-phase transformerless PV inverter.

This article is structured as follows. In Section 2, the configuration of proposed topology and selection of LCL filter parameters are described. Subsequently, the DC-link voltage balancing circuit converter is explained in detail in Section 3. The operation of proposed topology to generate constant common-mode voltage is discussed in Section 4. In Section 5, the experimental results on the leakage ground current performance, for both the introduced and conventional H-bridge topologies, are shown and discussed. Subsequently, comparative discussions on other aspects of the two topologies are presented in Section 6. Finally, the concluding remarks are given in Section 7.

## 2. CIRCUIT PARAMETER OF SC-HB TOPOLOGY

Figure 3 shows the circuit configuration of the SC-HB transformerless inverter topology. The performance of such an inverter is investigated with a symmetrical power circuit

| Parameter | Value |
|---|---|
| $L_{f1} = L_{f1n}$ | 3 mH |
| $L_{f2} = L_{f2n}$ | 2 mH |
| $L_b$ | 1 mH |
| $C_f$ | 2 $\mu$F |
| $C_{pv}$ | 100 nF |
| $C_{B1} = C_{B2}$ | 220 $\mu$F |
| $V_{PV}$ | 400 V |
| Switching frequency for balancing circuit and H-bridge inverter, $f_s$ | 8 kHz |
| Dead time, $t_d$ | 0.8 $\mu$s |

**TABLE 1.** Simulation and experiment parameters

($L_{f1} = L_{f1n}$, $L_{f2} = L_{f2n}$). The PV module is modeled as a DC voltage source for simplification. The simulation is performed using PSIM 9 (PowerSim Inc., Rockville, MD, USA), and the results are verified by a hardware prototype, the parameters of which are listed in Table 1. A dead time ($t_d$) of 0.8 $\mu$sec is chosen to avoid the DC link from being shorted during switching commutation. An LCL filter is placed at the output of the H-bridge inverter to suppress the switching harmonics and to provide better grid decoupling. The calculation of total filter inductance ($L$) is given in Eq. (2); the maximum ripple current ($\Delta_{ripple,max}$) was chosen to be 5–20% of the rated current [21]:

$$L = \frac{1}{8} \frac{V_{DC}}{\Delta_{ripple,max} f_{sw}}. \tag{2}$$

The configuration of an LCL filter with a split inductor has been used in the proposed topology, as shown in Figure 3. The filter inductor ($L$) is split equally between the line ($L_{f1}$) and neutral ($L_{f1n}$) branches to deal with the common-mode voltage of the converter [22]. Filter capacitance ($C_f$) is determinable by the reactive power rating, as expressed in Eq. (3), with $\alpha$ being the reactive power factor; its value is selected to be less than 5% [21]:

$$C_f = \frac{\alpha P_{rated}}{2\pi f_{line} V_{rated}^2}. \tag{3}$$

The filter capacitor ($C_f$) is placed in the middle of the inductors, partitioning the total inductance into two parts: $L_{f1}$ and $L_{f1n}$ at the inverter side and $L_{f2}$ and $L_{f2n}$ at the grid side. The relationship of $L_{f1}$ and $L_{f2}$ for the LCL filter is defined by Eq. (4), where $a$ is the inductance index of $L_{f1}$ and $L_{f2}$. The inductance index ($a$) can be calculated using the switching harmonic current attenuation ratio [23]. For stability reasons, $L_{f2}$ must be designed lower than $L_{f1}$ [24]. Equation (5) defines the resonant frequency ($\omega_{res, rad\ sec}$) for the LCL filter [24]. To avoid resonance effect and ensure carrier attenuation, filter resonance frequency ($f_{res}$) should be lower than switching frequency ($f_s$)

as described in Eq. (6):

$$L_{f1} = aL_{f2}, \tag{4}$$

$$\omega_{res} = \sqrt{\frac{L_{f1} + L_{f2}}{L_{f1}L_{f2}C_f}}, \tag{5}$$

$$f_{res} = \frac{\omega_{res}}{2\pi} < f_s. \tag{6}$$

## 3. THE BALANCING STRATEGY

In the adopted single-phase transformerless inverter topology, the leakage ground current ($I_g$) through PV parasitic capacitance ($C_{PV}$) can be reduced by connecting the midpoint of two series DC-link capacitors ($C_{B1}$ and $C_{B2}$) to the neutral point of grid, i.e., the system ground. However, series-connected capacitors may have non-uniform voltage distribution. The capacitor voltage balancing problem in the DC inverter link can be significantly reduced if the energy drawn from the each of the DC-link capacitors can be controlled. This can be done by
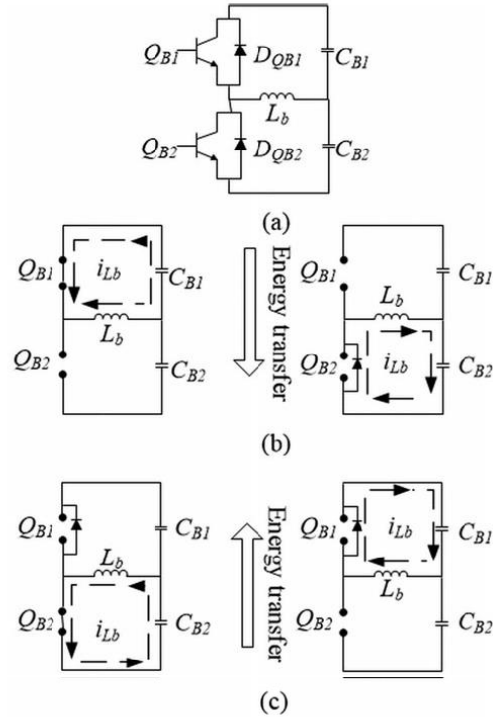


**FIGURE 4.** (a) Balancing circuit, (b) energy transfer from $C_{B1}$ to $C_{B2}$, and (c) energy transfer from $C_{B2}$ to $C_{B1}$.

using a simple balancing circuit [18], as shown in Figure 4(a). The balancing circuit has two switches ($Q_{B1}$ and $Q_{B2}$), which are operating in complement to one another, and one inductor $L_b$. By coordinating the switching of $Q_{B1}$ and $Q_{B2}$, the voltage across the DC link ($V_{DC}$) can be divided equally such that the voltage across $C_{B1}$ ($VC_{B1}$) is approximately equal to the voltage across $C_{B2}$ ($VC_{B2}$). The operation of the balancing circuit is explained next.

The voltage variation against the capacitor voltage is given by

$$\Delta V = VC_{B1} - VC_{B2}, \tag{7}$$

where $V_{CB1}$ and $V_{CB2}$ are the voltage across the upper and the lower capacitor, respectively.

A simple control method is implemented for the balancing circuit, which is derived from a buck-and-boost DC-DC converter. When $V_{CB1}$ is higher than $V_{CB2}$, *i.e.*, $\Delta V > 0$, $Q_{B1}$ starts operating within a specific ON-state duty cycle to maintain the DC-link voltage balance (see Figure 4(b)). Energy is transferred from upper capacitor $C_{B1}$ to lower capacitor $C_{B2}$ through inductor $L_b$ when $Q_{B1}$ is on. When $Q_{B1}$ is switched OFF, the energy stored in $L_b$ is released into $C_{B2}$ through the free-wheeling diode $D_{QB2}$. On the contrary, if $\Delta V < 0$ (when $V_{CB2}$ is larger than $V_{CB1}$), turning ON $Q_{B2}$ reverses the energy transfer from $C_{B2}$ to $C_{B1}$; see Figure 4(c). The energy is stored in $L_b$ when $Q_{B2}$ is on. When the $Q_{B2}$ is off, the energy in $L_b$ is transmitted into the $C_{B1}$ through $D_{QB1}$.

In the adopted topology, both voltage capacitors $C_{B1}$ and $C_{B2}$ are charged to half of the input PV voltage each through inductance $L_b$ and switches $Q_{B2}$ and $Q_{B1}$, as previously explained. To see the importance of the voltage balancing circuit, two simulations are conducted using the PSIM simulation package. First, the proposed inverter circuit is simulated without the balancing mechanism ($Q_{B2}$, $Q_{B2}$, and $L_b$ are excluded). Subsequently, the simulation is repeated for the case where the balancing mechanism is used together with the SC-HB inverter. The results are shown in Figures 5(a) and 5(b). For both simulations, the initial values of the series capacitor voltages, $V_{CB1}$ and $V_{CB2}$, are set arbitrarily to 225 and 175 V, respectively, to emulate the condition where $V_{CB1}$ and $V_{CB2}$ are unequal. The results in Figure 5(a) show that the capacitor voltages are unbalanced in the absence of a balancing circuit. With the balancing circuit, both series DC-link capacitor voltages are balanced and equal in the steady-state period, as shown in Figure 5(b).

## 4. LEAKAGE GROUND CURRENT REDUCTION IN SC-HB TOPOLOGY

Due to advantages offered by the unipolar SPWM switching technique in improving the quality of the injected inverter cur-
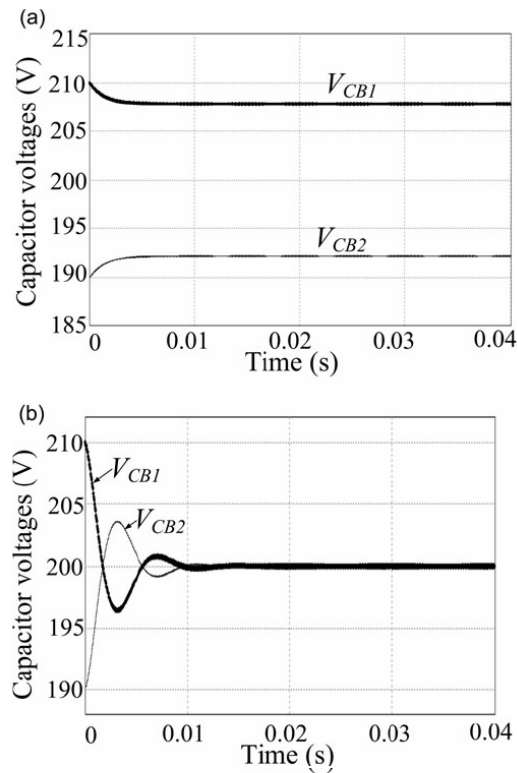


**FIGURE 5.** (a) Capacitor voltage ($V_{CB1}$) without balancing circuit and (b) capacitor voltage ($V_{CB1}$) with balancing circuit.

rent, this switching technique is used in the SC-HB topology. There are four states involved in the unipolar SPWM switching technique, *i.e.*, the zero positive state (state I), the positive active state (state II), the zero negative state (state III), and the negative active state (state IV). In the following explanations, operation of the first two states will be discussed. The other two states will not be explained, as state I's operation mode is similar to state III and the results of state IV are the same as state II except for different polarity of the inverter output voltage ($V_{ab}$). The summary of common-mode voltage ($V_g$) during all commutation in the proposed topology is illustrated in Table 2. In addition, the balancing strategy explained in Section 3 is implemented during all four states.

State I is applied by turning ON $Q_1$ and $Q_3$, as shown by the dotted lines of Figure 6(a). Meanwhile, state II is applied by turning ON $Q_1$ and $Q_4$, as shown by the dotted lines of Figure 6(b). In both figures, the balancing strategy operations are also highlighted. The solid lines represent the operation of