Broadband high performance laterally diffused metal–oxide–semiconductor power amplifier for mobile two-way radio applications

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Abstract: This paper highlights achievement of broadband high performance power amplifier (PA) line up for mobile two-way radio applications. In typical two-way radio applications the input radio-frequency signal to the first PA stage comes directly from the voltage controlled oscillator, with typically 3 dBm power. Owing to high output power requirement (~80 W) of mobile radio applications, up to three PA device stages are normally cascaded (pre-driver, driver and final PA stage). The key point in the design of the PA line up concerns the final stage. Here, this paper introduces a design methodology based on parallel-combined impedance matching technique (from theoretical derivation) enables the designers to develop broadband PA with actual PA device impedance (implementation of new generation laterally diffused metal–oxide–semiconductor device). Experimental results demonstrated output power of ~80 W and gain of 45 dB, while preserving efficiency of 55% over the bandwidth from 760 to 870 MHz. According to author's knowledge, this amplifier demonstrated highest efficiency with 13 V DC supply (operating at 80 W) in UHF broadband frequency with high gain operation (more than 45 dB) up to date.

1 Introduction

Modern mobile two-way radio communication must meet high performance and robustness criteria in the field. One of the key challenges in system architecture is the transmitter chain, specifically the power amplifier (PA) line up. In order to meet high performance and robust design, while minimising costs of the whole transmitter chain, power device selection and circuit topology should be carefully analysed. In typical two-way radio applications, a constant pre-defined envelope modulated radio-frequency (RF) signal (either frequency modulation or frequency shift keying) is injected directly from the voltage controlled oscillator (VCO) to the PA. Owing to low signal level from VCO (~3 dBm) and high output power requirements of the two-way radio product up to three PA device stages are normally cascaded, that si, the PA consists of pre-driver, driver and final PA stage. The key focus of this paper is the final PA design stage, particularly, final PA output impedance matching transformation having parallel combining technique [1, 2] (from analytical approach), followed by the design methodology employing source and load-pull technique [3, 4], and implementation of high power new generation laterally diffused metal–oxide–semiconductor (LDMOS) device technology. Practical design concept to meet thermal management is taken into consideration (heat-sink design) [5].

Bandwidth limitation in designing a broadband amplifier can be addressed through circuit design and device characteristics [6]. Broadband amplifiers need to be designed over a broad frequency range which indeed requires proper matching networks. This is to ensure a reasonable compensation for the variations of forward transmission S_{21} with frequency. Common techniques used to design broadband amplifiers are matching network compensation [7], negative feedback [8] and so on. Matching network compensation involves mismatching the input and output networks to compensate the changes with $|S_{21}|$, and the networks must provide the best input and output VSWR [4].

Large-scale RF and microwave power device production is actually based on silicon (Si), gallium arsenide, lateral diffusion (metal–oxide–semiconductor field-effect transistor) MOSFET (LDMOS) [9–12]. In addition, great research interest is devoted to high power density devices using wide-bandgap materials such as silicon carbide and gallium nitride (GaN) [13–16]. A higher bandgap corresponds to a higher breakdown field, which in turns implies the capability of the device to allow higher output voltage swings and thus attain higher output power levels. Moreover, high breakdown voltage results in larger output impedance values for a given current density, making the device matching easier for broadband applications [13]. Therefore the selection of high f_T–V_{bk} device technology is a good solution [13]. GaN devices offer a superior power density. Reasonable power can be obtained from comparatively small GaN devices with high source and load impedances and complexity of the matching networks can be reduced. However, they have the drawback of running with high supply voltage values. Typically 28 V or higher supply voltage will be used for GaN devices [16]. For mobile radio communications, 13 V is a favourable voltage due to the fact that the product can be used in automobile. In this regard, LDMOS would be an interesting choice. LDMOS technology is leading technology in base station and mobile radio communications [9–11, 17, 18].

In this work, a new prototype has been designed and fabricated with a demonstrated drain efficiency of 55% at operating power of 80 W for frequency range of 760–870 MHz. Note that three PA stages are cascaded (pre-driver, driver and final PA stage) and overall gain reported more than 45 dB across frequency. The final PA stage has been built with new high power LDMOS device technology process from Freescale Inc. Additional performance test such as stability and robustness are carried out in laboratory. Power amplifier (PA) is very stable and the transistor was not damaged by operating into 10:1 VSWR termination (with varying phase angle of the load termination). This amplifier demonstrated high energy conversion (high efficiency) with 13 V DC supply (operating at 80 W) in UHF broadband frequency. In addition, the amplifier requires small size area form factor and has a low cost implementation which is suitable to be integrated in mobile two-way radio applications.

2 Circuit principle

2.1 LDMOS characterisation and selection

To achieve broadband performance from a single ended PA device, the load impedance $R_{L,opt}$ must be close to ~50 Ω over wide frequency range

$$R_{L,opt} = \left[\frac{(V_{bk} - V_k)^2}{2P_{out}}\right] \quad (1)$$

where P_{out} is the output power from the device, where V_{bk} and V_k are breakdown and knee voltages, respectively. Therefore, scaling the device periphery is possible to achieve $R_{L,opt} \sim 50\ \Omega$ by means of DC voltage. However, this may imply lower output power. One can increase output power with the increase of DC voltage while keeping $R_{L,opt} \sim 50\ \Omega$. In this work, low DC supply of 13 V is selected because of the product design requirement. Therefore when PA device is running at 13 V (can be approximated to V_{bk}–V_k) and delivering P_{out} of 90 W, the $R_{L,opt}$ will be ~0.9 Ω. As a matter of fact, the design of a broadband frequency from 760 to 880 MHz (having loaded quality factor, Q_L of 2) with low DC supply and small $R_{L,opt}$, it is real challenge. As the result, impedance matching transformation network from $R_{L,opt}$ to 50 Ω termination will be complicated.

Owing to high output power requirement (~80 W) and using 13 V DC supply, there is no single ended LDMOS PA device available. However, new generation LDMOS device running with 13 V supply, new generation high power LDMOS device (n-channel enhancement lateral MOSFET)) from Freescale Inc. is employed [19]. Source and load pull characterisation are carried out, where best efficiency and output power of 70% and 43 dBm, respectively, are recorded over the entire desired frequency bandwidth (see Table 1). Indeed, the efficiency performance (at power of 45 W) of the device is high and combining two devices in parallel 80 W output power could be reasonable expected. One must take note that impedance matching transformation must be carefully considered here due to the fact that the overall impedance will be divided by half in parallel combination. The principle analysis will be discussed in the following subsection.

2.2 Output impedance analysis – design via source and load pull determination

Parallel-combining impedance matching [1] technique is introduced in this paper to achieve high output power while preserving high efficiency over the broadband frequency operating range. When two PA devices are placed in parallel configuration, both RF current generated from the devices must be carefully combined without having loading effect [19–21]. Let us consider i_1 and i_2 as the current source of each PA device, and $Z_a(\omega)$ and $Z_b(\omega)$ are the optimum output impedances of the PA device as a function of frequency (Fig. 1*a*). DC-RF conversion is assumed here, where RF output power of each device is generated from DC source as a function of frequency. One should take note that $Z_a(\omega)$ and $Z_b(\omega)$ are equal if the devices are identical. The following output voltage and current equations can be deduced from Fig. 1*a*

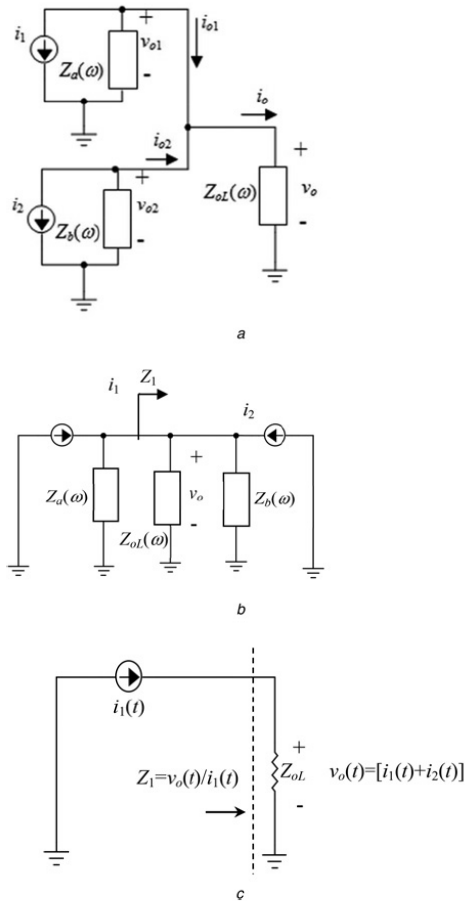

Fig. 1 *Output voltage and current equations can be deduced*

a Each current source is loaded with the output impedance, for example, $Z_a(\omega)$ and $Z_b(\omega)$, and terminated to single load $Z_{oL}(\omega)$

b Two current sources combining at a single output node

c Simplification of Fig. 3 for understanding of virtual impedance Z_1

$$i_o = i_1 + i_2 \quad (2)$$

$$v_o = v_{o1} = v_{o2} \quad (3)$$

Table 1 Summary of source and load-pull measurement characterisation of the new generation MV9 LDMOS device over the frequency of interest

Frequency, MHz	Drain voltage, V	I_{DQ}, mA	Optimum source impedance, Zs, Ω	Optimum source impedance, Z_L, Ω	P_{out}, dBm	Gain, dB	Efficiency, %
740	14	483	0.4–j1.2	1.2–j0.5	44.1	20.8	72.5
768	14	483	0.4–j1.4	1.2–j0.7	44.1	20.4	72.6
790	14	483	0.4–j1.5	1.2–j0.8	43.8	20.5	70.8
806	14	482	0.4–j1.6	1.2–j1.1	44.3	19.8	70.9
822	14	483	0.4–j1.8	1.2–j1.3	44.3	19.6	71.8
860	14	483	0.4–j2.0	1.2–j1.5	43.5	19.5	70.5

Performance is recorded at optimum performance; best efficiency at desired output power.

Therefore output RF power can be written as following

$$P_o = 0.5\{\text{real}(v_o \cdot i_o^*)\} \tag{4}$$

or

$$P_o = 0.5\{\text{real}((v_{o1}) \cdot (i_{o1} + i_{o2})^*)\} \tag{5}$$

In frequency domain, RF output power is given as following

$$P_o = 0.5\frac{v_{o1}^2}{\text{real}\{Z_{oL}\}} \tag{6}$$

or

$$P_o = 0.5[i_{o1} + i_{o2}]^2\text{real}\{Z_{oL}\} \tag{7}$$

where $Z_{oL}(\omega)$ is matched to the impedance terminated because of the present of $Z_a(\omega)$ and $Z_b(\omega)$, in which $Z_{oL}(\omega)$ typically is half of $Z_a(\omega)$ if the two PAs are identical.

From (7), to have maximum current combining i_o from i_1 and i_2 contributions, it is important that the magnitude and phase properties of i_1 and i_2 must be controlled with proper termination of $Z_{oL}(\omega)$. Let us analyse this in more details. Having two current sources in parallel with output impedances, as depicted in Fig. 1*b*, $Z_{oL}(\omega)$ is the result of injected current source at each active device output [19]. Fig. 1*c* is the simplification connection of two devices, represented each by the respective Norton current source and impedance, (i_1, $Z_a(\omega)$) and (i_2, $Z_b(\omega)$), respectively, and injecting their output in a common node, terminated by $Z_{oL}(\omega)$. Such equivalent description of the device output is valid up to moderate frequencies, where reactive effects (namely the device output reactance) can be neglected, thus considering a purely real output impedance.

Further, to a first approximation, $Z_a(\omega)$ and, $Z_b(\omega)$ may be neglected, assuming that the device loading effect is not significant when absorbed into the drain line. Such simplifying assumption can be, however, easily removed by absorbing the device output impedances into the $Z_{oL}(\omega)$, and will be adopted here for the sake of simplicity. The overall impedance loading each current source, because of the effect of the other injected sources, can be considered as virtual impedance [19].

The resulting current $i(t)$ through the load $Z_{oL}(\omega)$ is the sum of the two sources $i_1(t)$ and $i_2(t)$, represented as

$$i_1(t) = \Re\left\{I_1 e^{j(\omega t+\theta_1)}\right\} = I_1\cos(\omega t + \theta_1) \tag{8}$$

$$i_2(t) = \Re\left\{I_2 e^{j(\omega t+\theta_2)}\right\} = I_2\cos(\omega t + \theta_2) \tag{9}$$

where $\Re$ is the operator providing the argument's real part, I_1 and I_2 represent the magnitudes of the complex current sources and θ_1 and θ_2 are independent phase values. The virtual impedance Z_1 loading the i_1 current source can be obtained by looking into the common node with $i_2(t)$ in parallel with $Z_{oL}(\omega)$ [19]

$$Z_1 = \frac{v_o}{I_1 e^{j\theta_1}} = Z_{oL}\frac{\left(I_1 e^{j\theta_1} + I_2 e^{j\theta_2}\right)}{I_1 e^{j\theta_1}} = Z_{oL}\left[1 + \frac{I_2}{I_1}e^{j(\theta_2-\theta_1)}\right] \tag{10}$$

If there is no phase offset or in-phase combining (i.e. $\theta_2 = \theta_1$) is imposed in the DA, the virtual impedance Z_1 is real positive, then

$$Z_1 = Z_{oL}\left[1 + \frac{I_2}{I_1}\right] \tag{11}$$

From (11), to achieve optimum performance, one can explain that Z_1 is depending on the magnitude of the both current sources and Z_{oL} for the case of in-phase combining. In other words, the current source must be loaded with appropriate impedance and proper gate biasing to preserve efficiency and high output power operation (for FET devices).

One should take note that in practical application, $Z_a(\omega)$ and $Z_b(\omega)$ will not be considered as high impedance. However, this imply much lower as dictated in Table 1 (measured source and load impedance data). Therefore knowing the I_1 and I_2, and $Z_{oL}(\omega)$ properties from optimum power performance of the load pull measurement, Z_1 can be determined [22]. As explained before, $Z_{oL}(\omega)$ typically is half of $Z_a(\omega)$ or $Z_b(\omega)$ because of the identical PA device. As a result, the impedance matching network can be designed to transform from the current source of the PA device to $Z_{oL}(\omega)$.

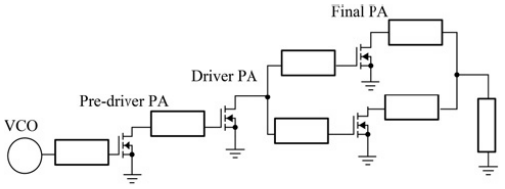

Fig. 2 *Complete PA architecture line up*

Direct matching technique will take place between pre-driver and driver PA, and driver PA to final PA
Output matching of final PA is the key focus

3 Design methodology for the final PA stage

Owing to parallel combining technique, two PA units of the new generation high power LDMOS devices are taken into consideration. The input drive signal from VCO is ~3 dBm. The overall PA line up architecture is highlighted in this paper, this consists pre-driver (H01 from Freescale Inc.) and driver stage (MRF1507 from Freescale Inc.) amplifiers as well. Both are LDMOS medium power devices. Therefore one can expect the operating gain of the PA line up can hit more than 45 dB. The PA architecture line is shown in Fig. 2. Direct matching technique was used for inter-stage matching between PA stages. The section will

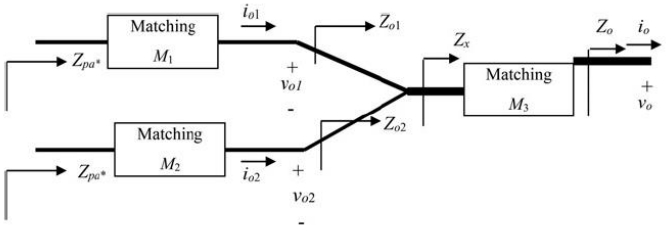

Fig. 3 *Impedance matching transformation of two devices in parallel*

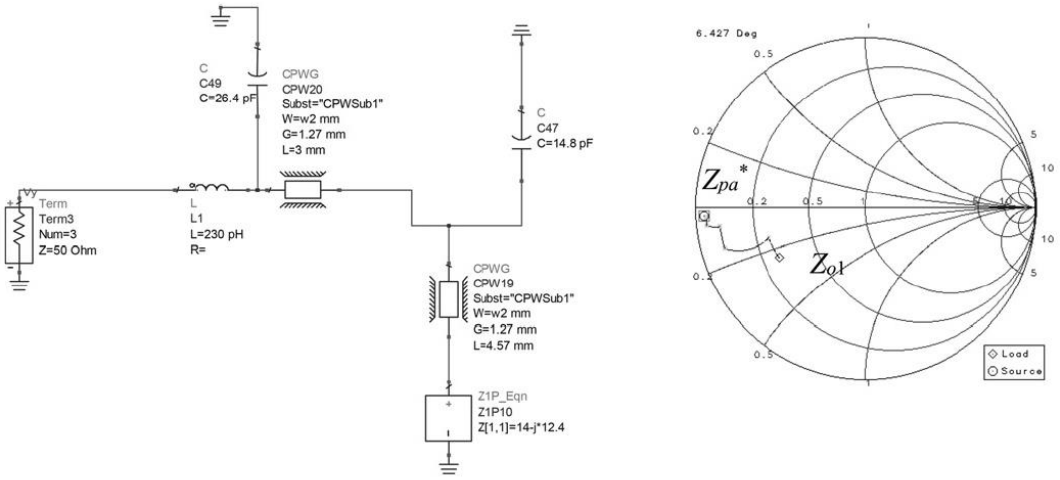

Fig. 4 *Mixed-lumped design elements for matching transformation from Z_{pa}*(ω) to Z_{o1} and graphical representation in Smith chart*

focus on the output final PA stage impedance transformation to 50 Ω load termination.

Design methodology with parallel-combine impedance matching technique will be discussed here, where two PA devices are placed in parallel configuration (refer to Fig. 3). Two primary impedance transformation networks are important, M_1 and M_3, since M_1 and M_2 are typically similar. The first network M_1 transforms from the PA optimum impedance Z_{pa}*(ω) to $Z_{o1}(\omega)$. $Z_{pa}(\omega)$* is the conjugate impedance determined from the load pull measurement (given in Table 1). For sake of simplicity, Z_{pa}*(ω) of 1.2 + j1.3 Ω

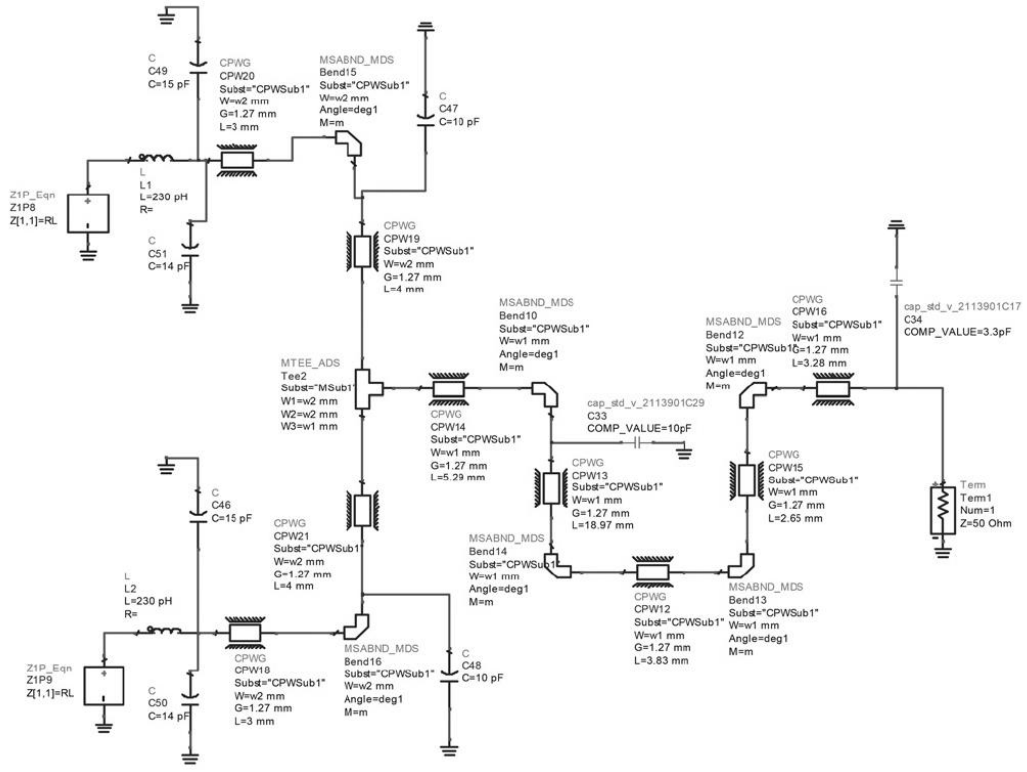

Fig. 5 *Complete matching transformation network from Z_{pa}*(ω) to 50 Ω termination*

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