Multilevel voltage source inverter with optimised usage of bidirectional switches

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Abstract: This study presents a multilevel voltage source inverter that has been designed to reduce circuit complexity by optimising the use of bidirectional switches. The proposed inverter is built by adding an auxiliary circuit comprising an arrangement of bidirectional switches to the three-phase, six-switch, full-bridge configuration. Several bidirectional switches are made to function in the optimised mode in which their operations are divided among the three phases. The presence of the optimised mode considerably reduces the number of power switches as the number of levels in the line-to-line voltage waveform increases. A novel modulation scheme based on space vector concept with virtual vectors utilisation has also been developed. A detailed study of the proposed inverter is described through the example of a five-level structure. The performance of the proposed inverter is analysed through MATLAB/SIMULINK simulation and verified via the practical tests conducted on a laboratory prototype with a DSP-based controller. A comparison is also made against classical multilevel inverters to complete the analysis.

1 Introduction

In recent years, multilevel inverters have played a considerable role in electronic power conversion for many industrial applications particularly in high-power range [1–3]. The successful penetration in high-power applications has motivated further studies on their potential presence for low-power applications as well [4]. This growing trend is as result of the superior characteristics of multilevel inverters which cannot be offered by the classical two-level inverters. For instance, multilevel inverters are able to produce voltage waveforms with better harmonic profile and lower total harmonic distortion (THD). This is owing to the presence of many voltage steps in the waveform that leads to a closer approximation to a pure sinusoid. This significant attribute paves the way for more advantages such as low dv/dt stress, few filter requirements and less switching loss [5–7].

Traditional multilevel inverters in the form of diode-clamped, flying-capacitor and cascaded H-bridge topologies have been widely studied over decades [8–13]. An important fact reached from these studies is the dramatic increase in the number of circuit's components as the number of voltage levels grows. For example, for a three-phase m-level inverter, diode-clamped topology requires $3(m-1)(m-2)$ clamping diodes, flying-capacitor topology needs $3(m-1)(m-2)/2$ flying capacitors and cascaded H-bridge topology uses $3(m-1)/2$ isolated DC sources. As a result, with increasing number of voltage levels, the circuit complexity becomes very high, the implementation cost is getting far from economical and the inverter's reliability issue raises the stake to emerge as a major concern. To overcome this issue, a number of methods have been proposed to increase the number of levels without a significant increase in the number of circuit's components. One approach uses unequal DC sources in the cascaded H-bridge inverter to form an asymmetric configuration [14–16]. Another approach is to use switched DC sources in generating many voltage levels through the combination of additive and subtractive values of the input DC supply [17, 18]. Combination of multilevel DC link with a single-phase full-bridge inverter has also been proposed as an alternative way to increase the number of levels [19]. Many forms of multilevel DC link supply have been suggested including switched series/parallel DC sources [20, 21]. As the abovementioned approaches have an obvious drawback from the fact that they still use isolated DC sources, multicell tolopogies have been introduced [22]. Although the number of DC sources can be reduced, the fact that the topologies use huge capacitor banks can make them unattractive [23]. Hybrid multilevel inverters have also been explored but they may pose a difficult challenge in providing complicated modulation techniques [24, 25].

Most of the proposed approaches are very much related to the cascaded H-bridge topology. This is mainly owing to the modularity feature that the topology offers. However, for asymmetric configurations, modularity is lost as the cells are not identical anymore. Regardless of this development, the diode-clamped inverter particularly the three-level

structure is still the one widely used in all types of industrial applications as the implementation cost is the most competitive [26, 27]. Thus, it is the purpose of this paper to focus on improving the characteristics and performance of the diode-clamped inverter by modifying its structure in order to give birth to a new multilevel inverter configuration. The improvement proposed in this paper is targeted at the reduction of the circuit complexity through the removal of clamping diodes. This in turn lessens the increase in power loss as the number of levels becomes bigger. Although active neutral-point-clamped multilevel inverter has been proposed to eliminate the use of clamping diodes, it comes at the expense of the use of more power switches instead [28]. As power switches are more expensive that diodes, the implementation cost of the inverter may consequently increase.

The proposed multilevel inverter carries some similarities to the diode-clamped inverter in the sense that both do not really need many isolated DC sources. The voltage balancing methods for the DC link capacitors that are used for the diode-clamped inverter can also be applied to the proposed inverter. Furthermore, in both inverters, the top outer and the bottom outer switches in each leg are responsible for the maximum and minimum voltage levels. Only the way that the other voltage levels are generated makes the proposed inverter different from the diode-clamped counterpart. The next section, Section 2 provides the general structure of the proposed inverter before a five-level inverter is illustrated. The operating principles of the five-level inverter with a novel modulation scheme are presented in Section 3. Section 4 details the results of the inverter's performance from simulation and experimental work whereas in Section 5, power loss analysis is given. Section 6 provides the comparison of the proposed inverter with other topologies especially the diode-clamped inverter before conclusions are drawn in Section 7.

2 Proposed topology

In this section, the proposed topology is introduced. The general concept employed that gives birth to the proposed topology is explained. As an illustration, the operation of the three-phase five-level configuration at low switching frequency is also presented.

2.1 General structure

Fig. 1*a* shows the generalised structure of the proposed topology which is basically derived from a three-level inverter presented in [29]. The structure is made up of three modules. Module 1 is the conventional full-bridge circuit whose switches are utilised to generate the maximum and minimum voltage levels in the line-to-line waveform. Module 2 is composed of three bidirectional switches in which each of them represents each phase. In other words, each switch functions in the normal mode in the sense that it is exclusively employed for a particular phase. Module 3 comprises a string of bidirectional switches which are connected to DC sources. The switches are made to operate in the optimised mode in a way that the operation of each switch is divided among the three phases. Here, only one switch is allowed to be active while others are turned off at a particular time. This is to avoid a short circuit across the DC sources. For m-level structure, the inverter requires $(m-2)$ bidirectional switches in Module 3. The appropriate interaction between Modules 2 and 3 produces the non-zero voltage levels in between the maximum and the minimum.

2.2 Five-level configuration

To illustrate the operation of the proposed topology, a five-level configuration is presented. Fig. 1*b* displays the five-level inverter. The inverter has 12 switches in which three bidirectional switches are used in Module 3 to produce nine voltage levels in the line-to-line voltage waveform of the following amplitudes: $-4V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, V_{dc}, $2V_{dc}$, $3V_{dc}$, $4V_{dc}$ and 0. In order to explain the basic operation of the inverter at low switching frequency for the generation of the line-to-line stepped voltage waveforms, 24 operational states are defined. The load currents are designated by i_A, i_B and i_C whose directions are given by the corresponding arrows in Fig. 1*b*. If any of the load currents follows the direction of the respective arrow, then its sign is positive and vice versa. Table 1 summarises the 24 operational states.

Out of the 24 operational states, six only require three switches in Module 1 to be active while other switches are turned off. These states lead to the maximum, the minimum and zero voltage levels. For example, referring to State 1, to obtain $V_{AB}=0$, $V_{BC}=-4V_{dc}$ and $V_{CA}=4V_{dc}$, Q_{A2}, Q_{B2} and Q_{C1} are turned on while other switches are turned off. This action connects node A and node B to ground, whereas node C is linked to $4V_{dc}$. As result, negative i_A, negative i_B and positive i_C are produced. For the remaining 18 operational states, four switches are made to be active: two active switches in Module 1, one active switch in Module 2 and one active switch in Module 3, while the others are off. These states generate all voltage levels other than zero. As an illustration, consider State 10 that produces $V_{AB}=3V_{dc}$, $V_{BC}=V_{dc}$ and $V_{CA}=-4V_{dc}$. Here, Q_{A1} and Q_{C2} from Module 1 are on, thus connecting node A and node C to $4V_{dc}$ and ground, respectively. The activation of Q_{B3} from Module 2 and Q_{S3} from Module 3 links node B to V_{dc}. This results in positive i_A, negative i_B and negative i_C.

3 Operating principles

Various modulation techniques have been used for multilevel inverters. These include those of low-frequency-based methods such as selective harmonic elimination [30] and space vector control [31]. Other competitive methods involve high switching frequency such as multicarrier pulse width modulation (PWM) [32]. In this work, one of the most preferred PWM strategy known as the space vector PWM [33] is employed. This section presents the description about how the space vector PWM is adapted for the proposed five-level inverter.

3.1 Switching states

To define the switching states, Fig. 1*b* is used as the reference. Consider one phase, say phase A. The switches involved with this phase are Q_{A1} and Q_{A2} from Module 1 and Q_{A3} from Module 2. All switches from Module 3 namely Q_{S1}, Q_{S2} and Q_{S3} are made for common use for the three phases as to optimise their usage. Here, V_{AO} is also used as the reference parameter to define the switching states. Let denote switching state for phase A as S_A. Through appropriate switching, the following are obtained:

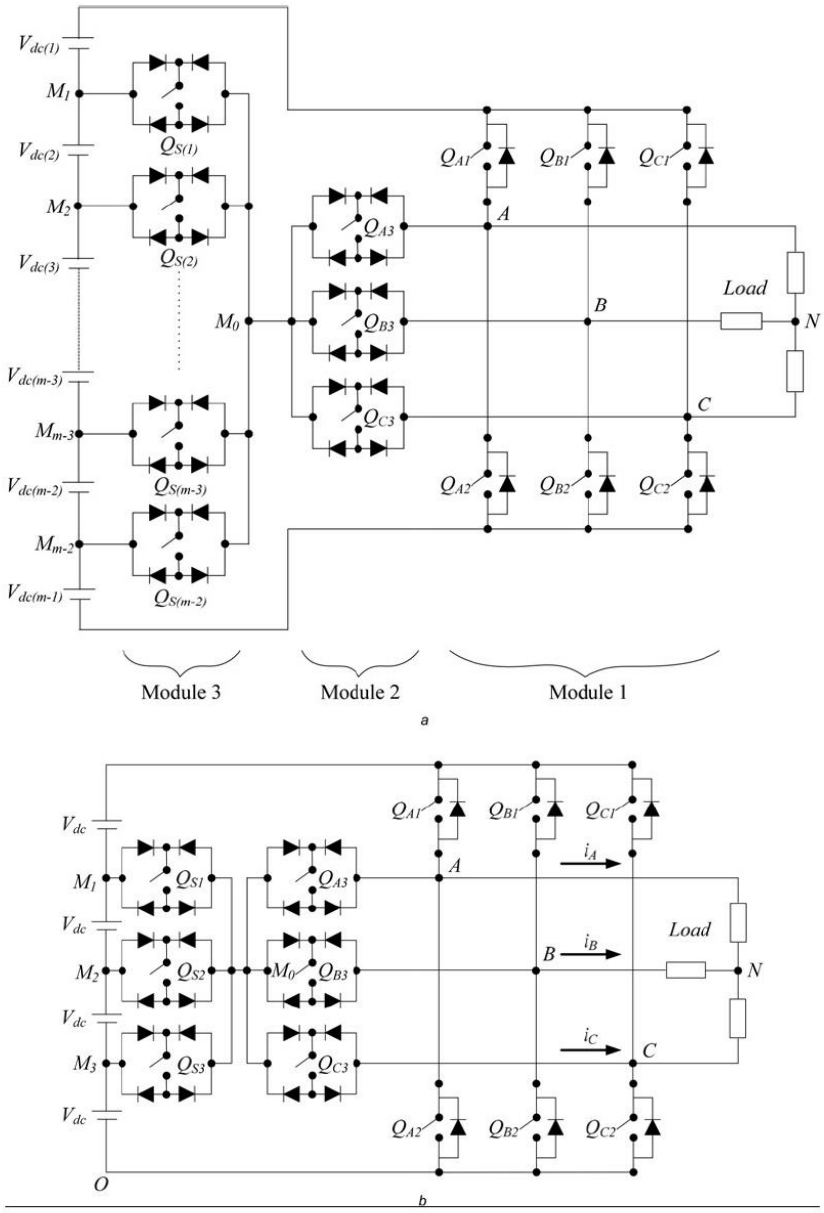

Fig. 1 *Proposed topology*

a Generalised structure
b Five-level structure

1. When Q_{A1} is switched on while others are switched off, V_{AO} becomes $4V_{dc}$.
2. When Q_{A2} is switched on while others are switched off, V_{AO} becomes 0.
3. When Q_{A3} and Q_{S1} are switched on while others are switched off, V_{AO} becomes $3V_{dc}$.
4. When Q_{A3} and Q_{S2} are switched on while others are switched off, V_{AO} becomes $2V_{dc}$.
5. When Q_{A3} and Q_{S3} are switched on while others are switched off, V_{AO} becomes V_{dc}.

By applying (1) below, five switching states are defined

$$S_A = \frac{V_{AO}}{V_{dc}} \tag{1}$$

Table 1 Operational states for the proposed five-level inverter to generate line-to-line stepped waveforms

Operational states	Active switches			Voltage levels			Current direction		
	Module 1	Module 2	Module 3	V_{AB}	V_{BC}	V_{CA}	i_A	i_B	i_C
1	Q_{A2}, Q_{B2}, Q_{C1}			0	$-4V_{dc}$	$4V_{dc}$	−	−	+
2	Q_{B2}, Q_{C1}	Q_{A3}	Q_{S3}	V_{dc}	$-4V_{dc}$	$3V_{dc}$	−	−	+
3	Q_{B2}, Q_{C1}	Q_{A3}	Q_{S2}	$2V_{dc}$	$-4V_{dc}$	$2V_{dc}$	+	−	+
4	Q_{B2}, Q_{C1}	Q_{A3}	Q_{S1}	$3V_{dc}$	$-4V_{dc}$	V_{dc}	+	−	+
5	Q_{A1}, Q_{B2}, Q_{C1}			$4V_{dc}$	$-4V_{dc}$	0	+	−	+
6	Q_{A1}, Q_{B2}	Q_{C3}	Q_{S1}	$4V_{dc}$	$-3V_{dc}$	$-V_{dc}$	+	−	+
7	Q_{A1}, Q_{B2}	Q_{C3}	Q_{S2}	$4V_{dc}$	$-2V_{dc}$	$-2V_{dc}$	+	−	−
8	Q_{A1}, Q_{B2}	Q_{C3}	Q_{S3}	$4V_{dc}$	$-V_{dc}$	$-3V_{dc}$	+	−	−
9	Q_{A1}, Q_{B2}, Q_{C2}			$4V_{dc}$	0	$-4V_{dc}$	+	−	−
10	Q_{A1}, Q_{C2}	Q_{B3}	Q_{S3}	$3V_{dc}$	V_{dc}	$-4V_{dc}$	+	−	−
11	Q_{A1}, Q_{C2}	Q_{B3}	Q_{S2}	$2V_{dc}$	$2V_{dc}$	$-4V_{dc}$	+	+	−
12	Q_{A1}, Q_{C2}	Q_{B3}	Q_{S1}	V_{dc}	$3V_{dc}$	$-4V_{dc}$	+	+	−
13	Q_{A1}, Q_{B1}, Q_{C2}			0	$4V_{dc}$	$-4V_{dc}$	+	+	−
14	Q_{B1}, Q_{C2}	Q_{A3}	Q_{S1}	$-V_{dc}$	$4V_{dc}$	$-3V_{dc}$	+	+	−
15	Q_{B1}, Q_{C2}	Q_{A3}	Q_{S2}	$-2V_{dc}$	$4V_{dc}$	$-2V_{dc}$	−	+	−
16	Q_{B1}, Q_{C2}	Q_{A3}	Q_{S3}	$-3V_{dc}$	$4V_{dc}$	$-V_{dc}$	−	+	−
17	Q_{A2}, Q_{B1}, Q_{C2}			$-4V_{dc}$	$4V_{dc}$	0	−	+	−
18	Q_{A2}, Q_{B1}	Q_{C3}	Q_{S3}	$-4V_{dc}$	$3V_{dc}$	V_{dc}	−	+	−
19	Q_{A2}, Q_{B1}	Q_{C3}	Q_{S2}	$-4V_{dc}$	$2V_{dc}$	$2V_{dc}$	−	+	+
20	Q_{A2}, Q_{B1}	Q_{C3}	Q_{S1}	$-4V_{dc}$	V_{dc}	$3V_{dc}$	−	+	+
21	Q_{A2}, Q_{B1}, Q_{C1}			$-4V_{dc}$	0	$4V_{dc}$	−	+	+
22	Q_{A2}, Q_{C1}	Q_{B3}	Q_{S1}	$-3V_{dc}$	$-V_{dc}$	$4V_{dc}$	−	+	+
23	Q_{A2}, Q_{C1}	Q_{B3}	Q_{S2}	$-2V_{dc}$	$-2V_{dc}$	$4V_{dc}$	−	−	+
24	Q_{A2}, Q_{C1}	Q_{B3}	Q_{S3}	$-V_{dc}$	$-3V_{dc}$	$4V_{dc}$	−	−	+

The same can be applied for phase B and phase C as well. By using subscript K to represent A, B and C, a generalised definition of switching states can be made. Table 2 details the derived switching states.

Switching states combinations in the form of $S_AS_BS_C$ can be generated by combining all the switching states of the three phases. The total allowable combinations is 65. To obtain the line-to-line and phase output voltages from given switching states, the following are derived

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = V_{dc} \begin{bmatrix} S_A - S_B \\ S_B - S_C \\ S_C - S_A \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2S_A - S_B - S_C \\ 2S_B - S_C - S_A \\ 2S_C - S_A - S_B \end{bmatrix} \tag{3}$$

3.2 Novel modulation scheme

In any space vector PWM scheme, the voltage vectors are obtained by transforming the voltage values in A-B-C frame into those of the α-β frame. This is done using Park's transformation [34] below

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} \tag{4}$$

The transformation results in the generation of 43 voltage vectors. Figs. 2*a* and *b* portrays the overall voltage vectors on α-β frame and the resulting hexagon, respectively. It appears that the vector hexagon is different from the normal five-level hexagon. Every sector consists of a large triangle in the middle and three small triangles at the three vertices which are separated between them by three trapeziums. This is as a result of the introduction of Module 3 in the proposed topology. The fact that each bidirectional switch in Module 3 operates in the optimised mode dictates that only one switch is turned on at any particular time as to avoid a short circuit across the DC sources. In the optimised mode, the operation of the switch that is turned on, is divided among phase A, phase B and phase C. Owing to that, switching states 1, 2 and 3 cannot exist at the same time. Therefore several switching states combinations are not allowed. For example, combination 310 is invalid because $S_A = 3$ and $S_B = 1$ occur simultaneously. This is not permitted since two bidirectional switches in Module 3 namely Q_{S1} and Q_{S3} are both active. The removal of invalid combinations leads to the elimination of six voltage vectors of magnitude $\sqrt{3}V_{dc}$ and 12 of magnitude $\sqrt{7}V_{dc}$.

The absence of the eliminated voltage vectors contributes to the problem of decomposing any given reference vector that falls in the trapezium. Here, four nearest vectors have to be considered and this requires at least four equations to determine the switching time of the four vectors. The conventional space vector PWM based on the three nearest vectors concept is not able to provide a solution since only three equations are involved. Therefore a new method is

Table 2 Switching states for the proposed five-level inverter

Switching states, S_K	Active switches			Voltage level, V_{KO}
	Module 1	Module 2	Module 3	
0	Q_{K2}			0
1		Q_{K3}	Q_{S3}	V_{dc}
2		Q_{K3}	Q_{S2}	$2V_{dc}$
3		Q_{K3}	Q_{S1}	$3V_{dc}$
4	Q_{K1}			$4V_{dc}$

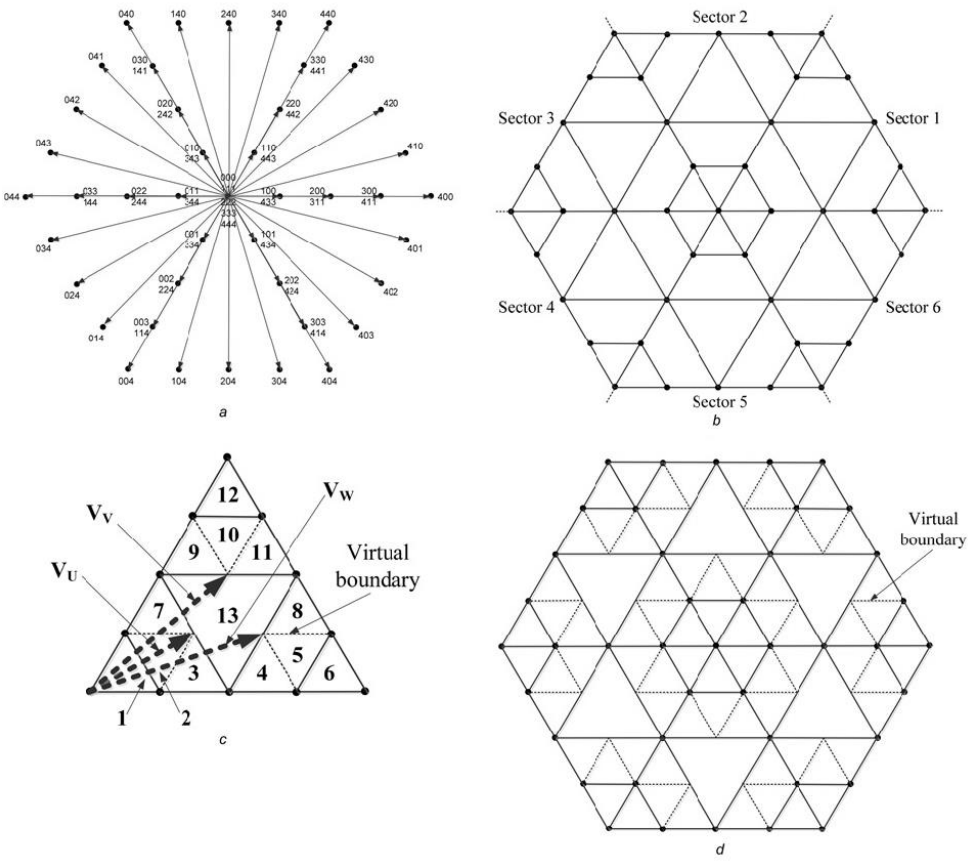

Fig. 2 *Space vector diagram for five-level structure based on the proposed topology*

a Voltage vectors
b Vector hexagon
c Virtual vectors in sector 1
d Resulting vector hexagon with virtual boundaries

introduced to simplify the representation of the reference vector in the trapezium. This is realised by using the virtual vectors. To describe the adaptation made, consider sector 1 of the vector hexagon as shown in Fig. 2*c*. Three virtual vectors V_U (amplitude of $\sqrt{3}V_{dc}$), V_V (amplitude of $\sqrt{7}V_{dc}$) and V_W (amplitude of $\sqrt{7}V_{dc}$) are introduced. Basically, the virtual vectors replace the vectors which are eliminated as a result of the invalid switching states combinations. The idea behind these virtual vectors is to break each trapezium in the sector into three triangles. This is done through the use of virtual boundaries which can be drawn by joining the virtual vectors to the opposite voltage vectors. By adopting this method, one large triangle in the middle and 12 small triangles can be formed including those created using the virtual boundaries. Any reference vector that falls in triangles 1, 6, 12 and 13 in Fig. 2*c* can be represented by a sum of different portions of the three nearest vectors that form the triangles. In other words, the conventional space vector concept applies. By denoting V_1, V_2 and V_3 as the three nearest vectors, then the corresponding switching time which are given as T_1, T_2 and T_3, can be determined by solving the following equations

$$V_{1,\alpha}T_1 + V_{2,\alpha}T_2 + V_{3,\alpha}T_3 = V_{\text{ref},\alpha}T_S \tag{5}$$

$$V_{1,\beta}T_1 + V_{2,\beta}T_2 + V_{3,\beta}T_3 = V_{\text{ref},\beta}T_S \tag{6}$$

$$T_1 + T_2 + T_3 = T_S \tag{7}$$

Here, V_{ref} is the reference vector, T_S is the sampling time and subscripts α and β refer to vector component in α-axis and β-axis, respectively.

However, if the reference vector lies in any of the other triangles namely triangles 2, 3, 4, 5, 7, 8, 9, 10 and 11, two nearest vectors are only considered to represent the reference vector. This is because of the fact that these triangles are formed using one or two virtual boundaries. The virtual vectors are not considered in the reference representation since its role is to only define the virtual boundaries in order to create the abovementioned triangles. To calculate the switching time of the two nearest vectors, adaptation of the three nearest vector concept is done by removing the term related to the third nearest vector in

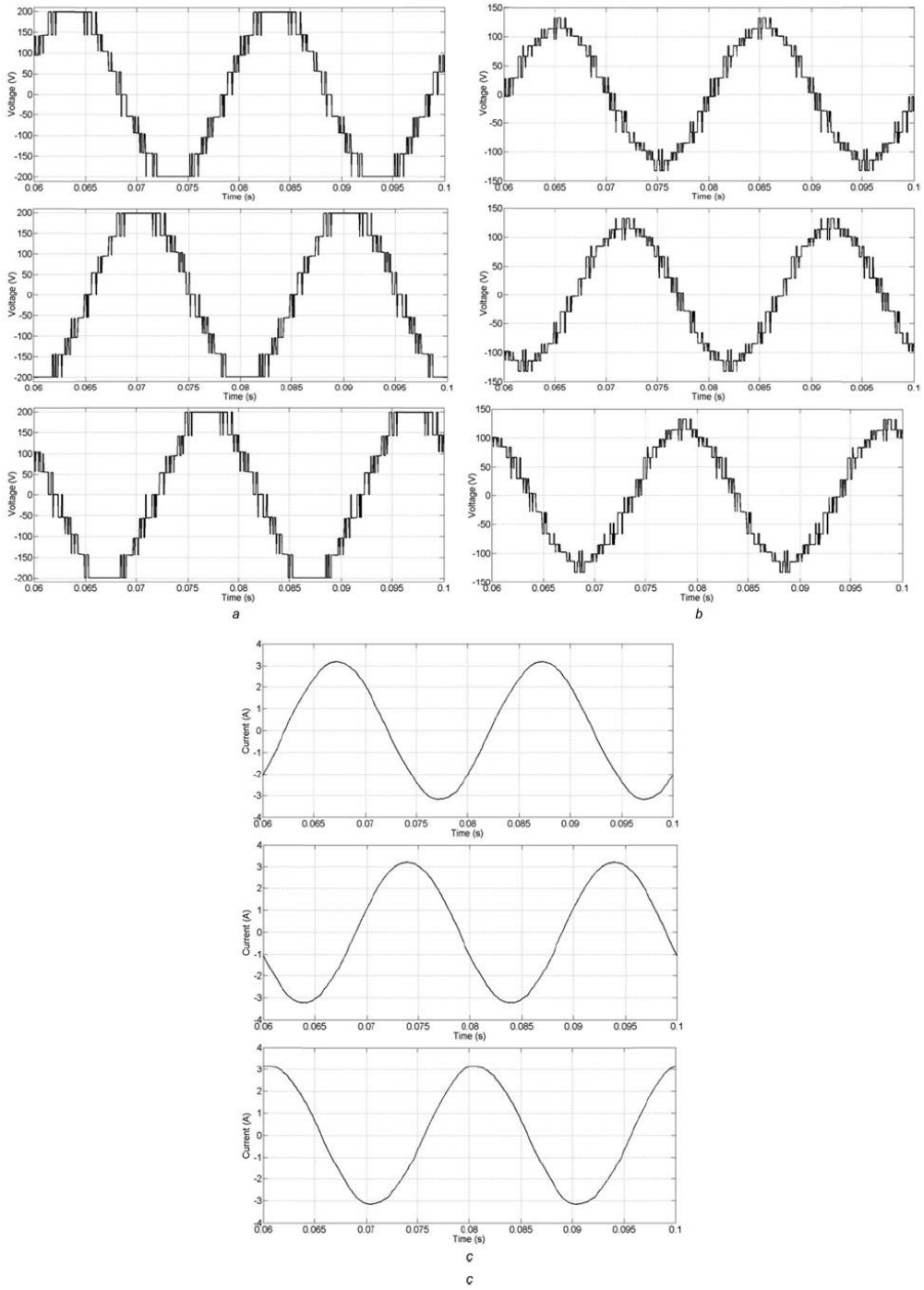

Fig. 3 *Simulation results for the proposed five-level inverter waveforms*

a Line-to-line voltages
b Phase voltages
c Load currents

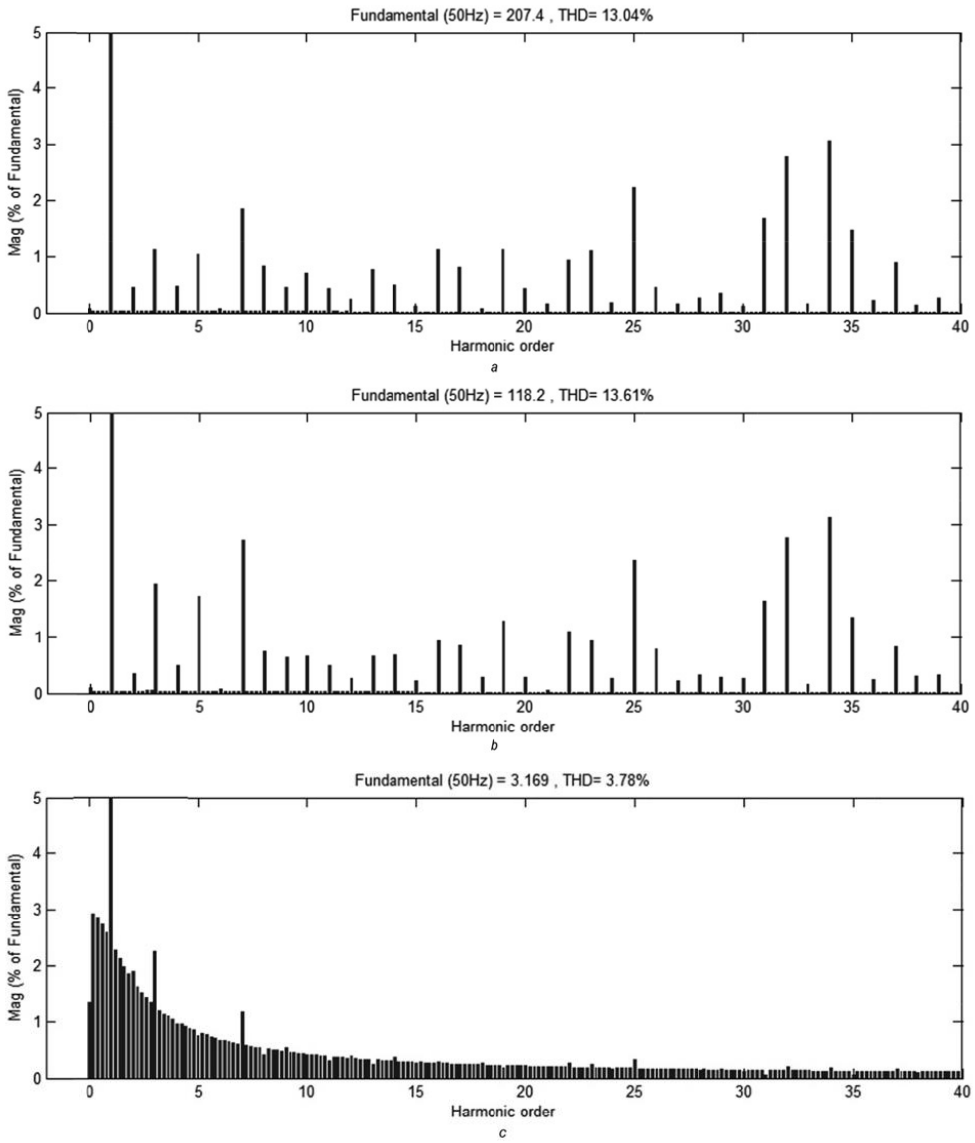

Fig. 4 *Simulation results for the proposed five-level inverter harmonic spectra*

a Line-to-line voltage
b Phase voltage
c Load current

(5)–(7) to derive the following equations

$$V_{1,\alpha}T_1 + V_{2,\alpha}T_2 = V_{\text{ref},\alpha}T_S \tag{8}$$

$$V_{1,\beta}T_1 + V_{2,\beta}T_2 = V_{\text{ref},\beta}T_S \tag{9}$$

$$T_1 + T_2 = T_S \tag{10}$$

By using (8), (9) and (10), T_1 and T_2 can be solved by either using the values in α-axis only or the values in β-axis only. For solution using α-axis only, (8) and (10) are used while (9) and (10) are applied when the values in β-axis are considered. To avoid confusion, T_1 and T_2 are rewritten as $T_{1,\alpha}$ and $T_{2,\alpha}$ for solution using α-axis only and as $T_{1,\beta}$ and $T_{2,\beta}$ for solution using β-axis only. Hence, the following are obtained

$$T_{1,\alpha} = \frac{V_{\text{ref},\alpha} - V_{2,\alpha}}{V_{1,\alpha} - V_{2,\alpha}} T_S \tag{11}$$

$$T_{2,\alpha} = T_S - T_{1,\alpha} \tag{12}$$

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