Semi-Z-source inverter topology for grid-connected photovoltaic system

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Abstract: Transformer-less inverters are necessary parts for grid-connected renewable energy resources. Owing to its cost effectiveness, downsize and less weight, great attention has been paid to these inverters development. With these aforementioned advantages, these inverters have limitations like the flow of leakage current through photovoltaic arrays, high total harmonic distortion (THD) at inverter's output and DC current injection to the grid. This study presents coupled inductor-based single-phase transformer-less semi-Z-source inverter topology to lessen those limitations. Since the DC input and AC output voltage share a common ground, the presented inverter system is categorised under doubly grounded topologies. For the purpose of handling, the non-linearity of the voltage gain of semi-Z-source inverter, a non-linear sinusoidal pulse-width modulation technique has been employed. The prototype of the suggested inverter has been constructed. The performance and compatibility of modulation technique are verified under different loading conditions. The feasibility of the configuration is ensured based on the mitigated common-mode leakage current, the substantially lower THD as well as DC current injected to the grid. Moreover, the presence of coupled inductor significantly contributes in reducing input current ripple, installation area of the inverter and enhancing the efficiency. Finally, this topology exhibits appreciable performance to operate synchronously and transfer power to the grid.

1 Introduction

Renewable energy resources (RERs), like wind turbine, solar photovoltaic (PV) and fuel cell are becoming more and more popular in recent era. This is because of the increasing demand of the clean energy, rapid development of rural area and the concern regarding environmental pollution around the world. As a result, power supplied to the utility grid, especially single-phase low-power systems (≤5 kW) from RER is demanding. These RERs are only capable of producing DC voltage at the output, while to connect these RER with grid, these require AC voltage at the output. Therefore inverters are required to place in between RER and grid to regulate power conversion and control optimisation [1, 2].

Isolated and non-isolated inverters are widely used for connecting RERs with utility grid. The problems of using these isolated inverters are not only the high system cost and larger system size but also reduced overall efficiency of the system. The reason behind these disadvantages is the presence of transformers in the system with line or high frequency for electrical isolation [3]. In contrast, use of non-isolated inverters reduces both cost and size along with improved system efficiency. Presently, the requirement of galvanic isolation is almost obsolete from low-voltage utility grid. Hence, transformerless inverters have turned into the market mainstream [4–6]. However, transformerless systems require some safety issues to be considered, like minimisation of connection effect between the input DC source and the grid as well as DC current injection to the utility grid. If same ground is not shared by both the PV cell and the grid, a variable common mode voltage is developed. As a result, large common-mode leakage current may flow through the parasitic capacitor between PV array and the ground which in turns, reduces the current quality of the grid, rises the system losses and induces electromagnetic interference (conducted and radiated) [6–9].

Conventionally, half or full-bridge inverters have been used to mitigate the problem of common-mode leakage current using bipolar sinusoidal pulse-width modulation (SPWM). So that, no variable common mode voltage is generated. However, half-bridge inverter requires approximately more than 700 V of the DC voltage to produce 220 V_{ac} at the output. Hence, series connections of large number of PV arrays or high conversion ratio DC–DC converter are required. On the other hand, the full-bridge inverter topology requires 50% of the input voltage than that of half-bridge topology (approximately greater than 350 V for 220 V_{ac}) [9]. However, the disadvantages of full-bridge inverter topology are high-current ripple, lower efficiency and large filter inductor. Another way to solve the common-mode leakage current problem is to use doubly grounded topologies. The advantages of these topologies are simple circuit design, low investment cost and enhanced safety [6, 7, 10]. Hence, in this paper, preference has been given to the doubly grounded transformerless topology.

On the contrary, some operational issues also need to be taken into consideration for transformerless grid connected

systems in order to maintain power quality. Such operational issues contain total harmonic distortion (THD), output current regulation and DC current injection. The IEEE and the IEC standards have provided some limit on the maximum range of THD and injected DC current [11, 12]. Acute attention is needed for the DC current injection because this may flow through distribution transformer, energy meters and residual current devices [13–15]. Otherwise, DC current cause saturation to distribution transformer, decrease the efficiency of the system, error in the measurement of energy meter and protective equipment starts malfunctioning. The standard values of DC current injection are different around the world. This limit varies from 5 mA to 1 A where 5 mA is for UK and 1 A for Germany [16, 17]. In contrast, the limit of DC current injection is 0.5% of the rated output current of the inverter for USA and 1% of the rated output current of the inverter for Japan [11, 12].

On the other hand, enhancement of the performance of these transformerless inverters is possible by designing the passive components of the inverter. Most importantly, inductor design is important to improve the performance. It is found that choosing of coupled inductor than separated inductor is best choice for the betterment of inverter performance [18–23]. Also, the role of coupled inductor is very significant in the modern high-frequency switching inverters topology. Since, coupled inductors have the ability to reduce the input current ripple, output voltage ripple and minimise the inverter size. Moreover, the inverter that contains coupled inductor can respond faster to load transient and can decrease the output decoupling capacitance. As coupled inductor minimises the ripple current, it can also minimise the core loss [18–23].

To improve the performance and lessen the cost, many transformerless inverter topologies based on traditional inverter and Z-source or quasi-Z-source inverters have been presented and analysed for renewable energy distributed generators especially for PV application in [14, 24–35]. Doubly grounded features are not included in most of these topologies. Recently, in [36], semi-Z-source inverter for single-phase PV system has been proposed, which shows the ground sharing option between grid and inverters. However, in [36], only the working principle of semi-Z-source inverter with respect to resistive load has been presented. Although, it is mentioned that, this inverter is applicable to incorporate solar PV to utility grid, but the results of grid tie application has not presented in [36]. In addition, the power quality issues during grid connected application like THD and DC current injection have not expressed. Also the features of coupled inductors technique have not illustrated. Another study in [37], discussed about three-switch three-state single-phase Z-source inverter topologies. However, the performance of the inverter under different loading conditions along with the analysis of THD and DC current injection has not included in [37].

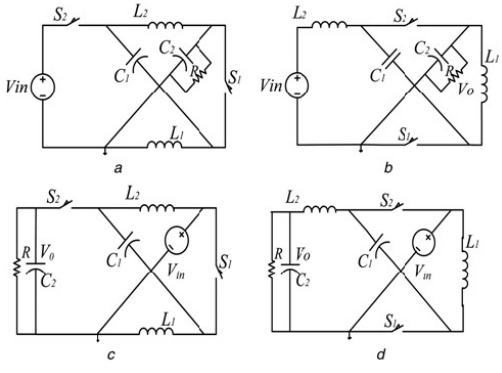

Fig. 1 *Discontinuous voltage gain and Continuous voltage gain*
a, *b* Z-source and quasi-Z-source DC–DC converters
c, *d* Z-source and quasi-Z-source DC–DC converters

A single-stage transformerless semi-Z-source inverter topology for grid connected application is presented in this paper by considering coupled inductor technique. The benefit of this semi-Z-source inverter topology over traditional single-phase full-bridge inverters and Z-source or quasi-Z-source inverters is, to generate sinusoidal voltage at the output of semi-Z-source inverter needs only two switches. Beside this, it contains Z-source network in AC side of the semi-Z-source network, which is different from conventional topology and results in size minimisation. The feasibility of the inverter topology has been analysed not only for static load like *R*, *R–L* but also for dynamic load like single-phase induction motor and grid. This inverter aims to minimise the common-mode leakage current with its ground sharing features. It also ensures less THD and DC current injections to the grid by utilising the coupled inductor techniques. In addition, the presented semi-Z-source inverter topology maintains appreciable DC to AC conversion efficiency compared with the conventional inverter and semi-Z-source inverter in [36] by utilising the coupled inductor techniques. On the contrary, the coupled inductor contributes in minimising size of the inverter. To generate sinusoidal voltage at the output, it uses the non-linear sinusoidal voltage gain curve as voltage reference. For this, a non-linear SPWM technique is used to obtain necessary control signal to generate sinusoidal voltage.

Section 1 contains an introduction specifying the rational of the project described in this paper. Basic principles of the transformerless semi-Z-source inverters are briefly described in Section 2 followed by the modulation principles in Section 3. Section 4 provides required equations for design. Section 5 describes the important details of experimental setup as well as the results obtained and their discussion. Also this section shows the distortion factor enquiry followed by power losses and efficiency analysis. At last, Section 6 includes the conclusion drawn from all the above discussed section.

2 Basic principle of transformerless semi-Z-source inverter

Topologies of the DC–DC converters of Z-source and quasi-Z-source are shown in Fig. 1 with the ground sharing nature [30]. Discontinuous voltage gain curve for converters of Figs. 1*a* and *b* are shown in Fig. 2*a*. While, Fig. 2*b* shows the continuous voltage gain curve of the topologies shown in Figs. 1*c* and *d*. Alternating (positive and negative) voltage can be generated by all these topologies at the output when duty ratio varies in between 0 and 1. However, generation of positive and negative voltages at the output with continuous voltage gain curve can be done only by the topologies shown in Figs. 1*c* and *d*. Hence, with appropriate modulation strategy these two topologies can be used as inverter as like as the traditional full-bridge inverter. This inverter can generate voltages between $-V_{in}$ to $+V_{in}$ at

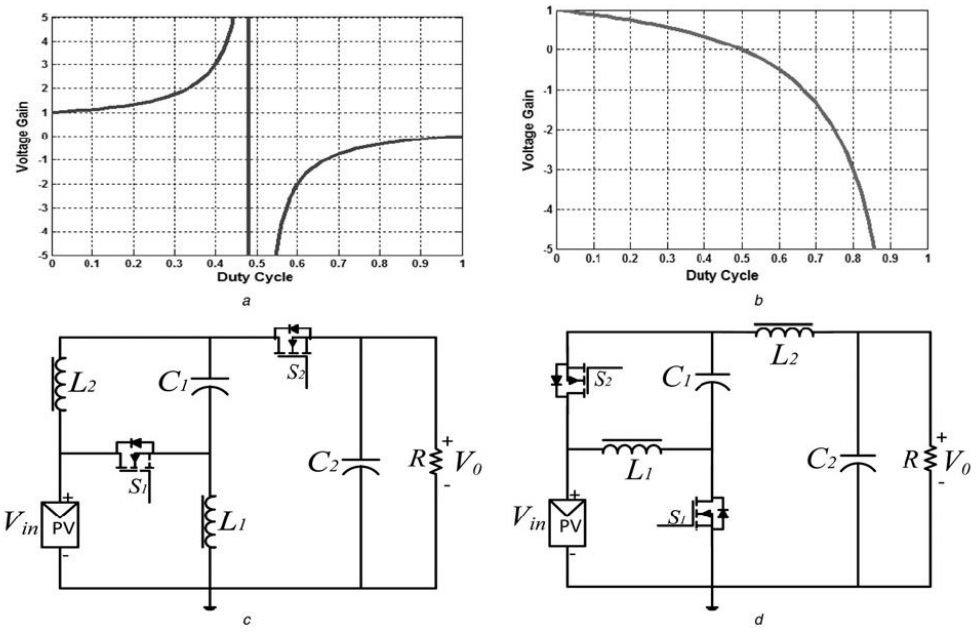

Fig. 2 *Discontinuous voltage gain, continuous voltage gain curves and single-phase semi-Z-source inverters*

a Discontinuous voltage gain curve of Z-source and quasi-Z-source DC–DC converters
b Continuous voltage gain curve of Z-source and quasi-Z-source DC–DC converters
c, *d* Single-phase semi-Z-source inverters

the output while the duty cycle changes remains in between 0 and 2/3.

Based on the aforementioned discussions, topologies of the single-phase semi-Z-source inverters with coupled inductor are shown in Figs. 2*c* and *d*. From the duty cycle against voltage gain curve shown in Fig. 3*a*, it is clear that when the duty cycle of switch S_1 varies from 0 to 1/2, the inverters can provide positive voltage at the output, whereas, from 1/2 to 2/3 the output voltage is negative [36]. For the duty cycle of 1/2, the inverter produces zero voltage at the output. Figs. 3*b* and *c* show the two states of operation, respectively. In state I, switch S_1 conducts where input voltage source and capacitor C_1 charge the two inductors. For state II, switch S_2 conducts and two inductors have turned into sources.

The direction of current references of the inductor and the voltage references of the capacitor are mentioned in Figs. 3*b* and *c* for the following steady-state equations. Details of the modes of DC operation are shown in [30]. The steady-state equations can be derived based on inductor voltage-second balance and capacitor charge balance principle. The steady-state equations are as follows

$$\frac{V_o}{V_{in}} = \frac{1-2D}{1-D} \tag{1}$$

$$V_{C_1} = \frac{D}{1-D} V_{in} \tag{2}$$

$$I_{L_2} = -I_o \tag{3}$$

$$I_{L_1} = -\frac{D}{1-D} I_o \tag{4}$$

If it is assumed that, inverter output voltage is (5) then the modulation index can be expressed as in (6). Equation (7) has been derived from (1), (5) and (6). $D' = 1–D$, the duty cycle of switch S_2, which can be expressed as (8)

$$V_o = V \sin \omega t \tag{5}$$

$$M = \frac{V}{V_{in}} \tag{6}$$

$$D = \frac{1 - M \sin \omega t}{2 - M \sin \omega t} \tag{7}$$

$$D' = \frac{1}{2 - M \sin \omega t} \tag{8}$$

3 Semi-Z-source inverters modulation principle

Traditional full-bridge inverter has straight line relation between duty cycle and voltage gain. For this reason, to generate sinusoidal voltage at the output SPWM technique is used. However, there is a non-linear relation between voltage gain and duty cycles of semi-Z-source inverters. For this reason, a non-linear SPWM is used to generate sinusoidal wave as shown in Fig. 3*d* [36]. A derived reference voltage is shown in (8) to control the duty cycle of switch S_2. To turn on switch S_2, it is necessary the reference value should be greater than carrier value. Equation (7) shows the reference signal of S_1, which is complementary of S_2 and the range of the modulation index is between 0 and 1. Fig. 3*d* shows the switching signals of

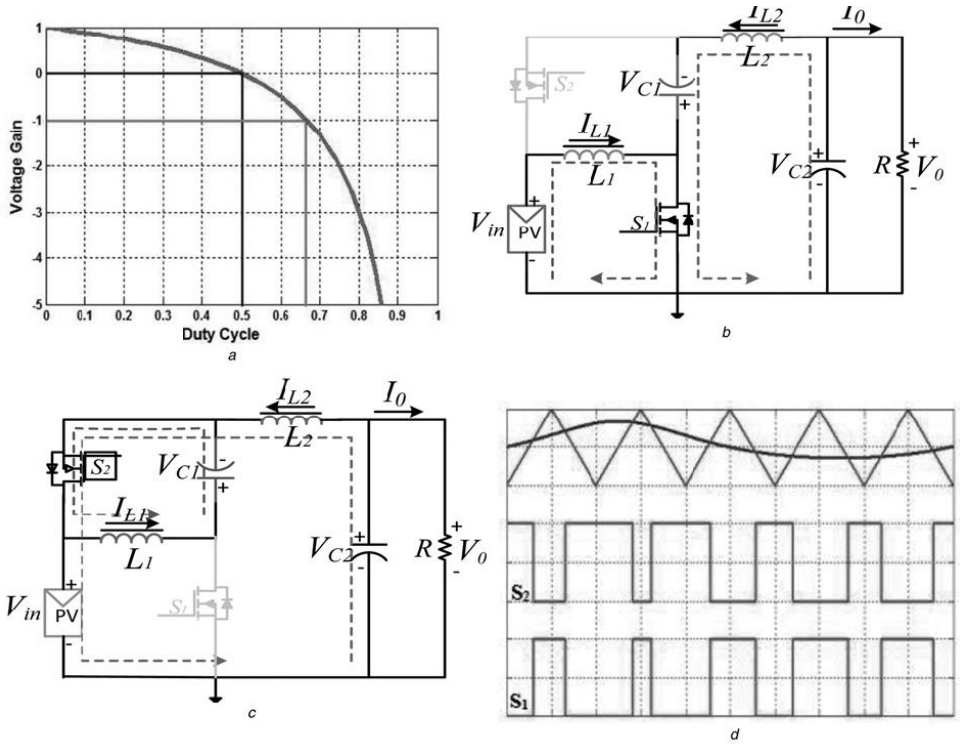

Fig. 3 *Semi-Z-source inverters*

a Voltage gain of single-phase semi-Z-source inverters
b Modes of operation of semi-Z-source inverters at state I
c Modes of operation of semi-Z-source inverters at state II
d Modulation methods of semi-Z-source inverters

the switches S_1 and S_2 at the time when the modulation index is 2/3.

4 Design and analysis of the circuit parameter

Configuration of semi-Z-source inverter shown in Fig. 2*d* has been chosen to analyse various parameters and design consideration of the circuit component. Let the output current expressed in (9) is in phase with output voltage. Voltage across the switch during the OFF state and current through the switch during the ON state can be presented like (10) and (11). From (10) and (11), the maximum OFF state voltage across the switch and maximum ON state current through the switch can be calculated. For this inverter topology, although the switches need to withstand a high voltage it can be applied with high-voltage silicon carbide (SiC) switches [38, 39]

$$I_o = I \sin \omega t \tag{9}$$

$$V_S = V_{in} + V_C = \frac{1}{1-D} V_{in} = (2 - M \sin \omega t) V_{in} \tag{10}$$

$$I_S = I_{L_1} + I_{L_2} = -\frac{1}{1-D} I_o = -(2 \sin \omega t - M(\sin \omega t)^2) I \tag{11}$$

Voltage across capacitor C_1 and current through inductor L_1 can be stated by (12) and (13), which are derived from (2), (4), (7) and (9). Voltage ripple of the capacitor C_1 and the current ripple of the inductor can be dictated by (14) and (15) considering $L_1 = L_2$. Now, from (12) and (14), the value of capacitance C_1 and from (11) and (13), the value of inductance L_1 can be selected considering the peak ripple requirement of the voltage and current, respectively. Owing to page limit, details of the design procedure has not provided here. For detail design procedure, one can go through [36]

$$V_{C_1} = \frac{D}{1-D} V_{in} = (1 - M \sin \omega t) V_{in} \tag{12}$$

$$I_{L_1} = -\frac{D}{1-D} I_o = -(\sin \omega t - M(\sin \omega t)^2) I \tag{13}$$

$$\Delta V_{C_1} = \frac{(1-D) T_s I_{L_1}}{C_1} = \frac{-\sin \omega t + M(\sin \omega t)^2 \, T_s I}{(2 - M \sin \omega t) C_1} \tag{14}$$

$$\Delta I_{L_1} = \Delta I_{L_2} = \frac{V_{in} T_s D}{L_1} = \frac{V_{in} T_s (1 - M \sin \omega t)}{L_1 (2 - M \sin \omega t)} \tag{15}$$

5 Experimental design

For the purpose of experimental validation, a prototype rated 48-W, 50 Hz transformerless semi-Z-source inverter is constructed according to the diagram shown in Fig. 2*d*. The constructed laboratory prototype model of the transformerless semi-Z-source inverter system is shown in Fig. 4. The input voltage of this prototype is about 50 V and the output voltage is about 35.35 V. The switching frequency of this system is 50 kHz. Here, for the prototype, two MOSFETs (STP75NF20) are chosen as switches. The values of both the capacitors C_1 and C_2 are 4.7 µF considering voltage ripple is limited to 5.75% of the peak voltage across the capacitors. For the prototype, polyester film capacitors (MPE475 K) are chosen. Performance real-time target machine (SPEEDGOAT) has been used to produce the switching signals for the inverter.

As mentioned earlier, the most essential components for semi-Z-source inverter are inductor that not only protect the input voltage source but also limit the input current ripple of the inverter. Inductor also serves the purpose of output filter. Two inductors (L_1 and L_2) used in semi-Z-source inverters can be placed in a single core or in two different cores. To minimise the input current ripple and to reduce the size, coupled inductor method is chosen for the prototype by ensuring identical current flow. For high frequency operation, ferrite materials have the low loss feature and for this, magnetic core of ferrite materials (45528EE) is chosen for this prototype. To prevent the inductor core from saturation under load, an air gap is used within the core structure because; the energy is being stored in air gap, which will prevent the core from saturation under load. The values of the inductor L_1 is 400 µH considering current ripple limited to 1/3 of the peak current of the inductor. The values of the inductor L_2 is also 400 µH that can be calculated by the same procedure. Finally, the THD of the output voltage and current has been analysed using YOKOGAWA WT 1800 precision power analyser.

Experimental results of the laboratory prototype model of 48-W transformerless semi-Z-source inverter are shown in Figs. 5–10. The prototype has been tested under *R* load, *R–L* load and motor load. During the laboratory experiment, about 50 V input voltage has been applied and the modulation index has been fixed to 0.95. Around 27 Ω resistance and 285 mH inductance have been used as load. Also, a single-phase induction motor (1/4 Horse power, 50 Hz, 220 V, 2.84 A and RPM-1450) from Mitsubishi Electric has been used as load.

Experimental results for *R* load are shown in Fig. 5. Fig. 5*a* shows the gate to source voltage V_{GS1} of switch S_1, drain to source voltage V_{DS1} of switch S_1, output voltage V_o and output current I_o during *R* load condition. Zoomed version of Fig. 5*a* is depicted in Fig. 5*b*. V_{GS1} and V_{DS1} of switch S_1 are operating in completely reverse according to the given figures. In addition, there is no phase difference between output voltage and output current. Moreover, output voltage polarity changes with the change of duty cycle of the switch, which satisfies the theoretical background. Drain to source voltage V_{DS1} of switch S_1, drain to source voltage V_{DS2} of switch S_2, output voltage V_o and output current I_o are shown in Fig. 5*c*. Fig. 5*d* represents zoomed view of Fig. 5*c*. It can be said that, like the theoretical background these two switches are operating in complementary manner with 50 kHz switching frequency and maximum off state voltage across the switches are 150 V.

Fig. 6 illustrates the experimental results for *R–L* load. When *R–L* have been considered as load, except for output current and voltage the remaining results are almost same like *R* load. It observed from Figs. 6*a* and *c* that the output current is lagging the output voltage and the magnitude of the output current decreases as the load increase.

Waveforms of input voltage V_{in}, voltage across capacitor C_1, output voltage V_o and output current I_o for *R* and *R–L* loads are shown in Figs. 7*a* and *b*, respectively. These two figures illustrate that, peak capacitor voltage is twice the input voltage for both the *R* and *R–L* loads. Moreover, both the positive and negative peak values of the output voltage are equal to the input voltage. Furthermore, during experiment the input voltage has been measured between DC + terminal and ground for both the *R* and *R–L* loads.

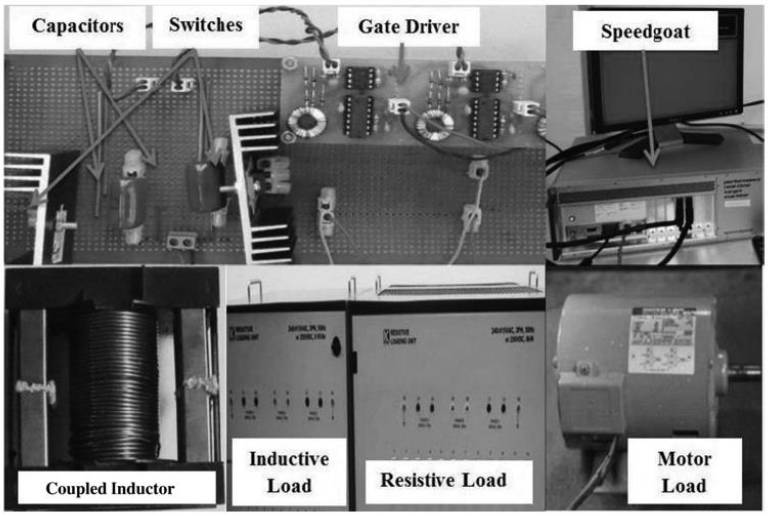

Fig. 4 *Most important components of the experimental setup of semi-Z-source inverter*

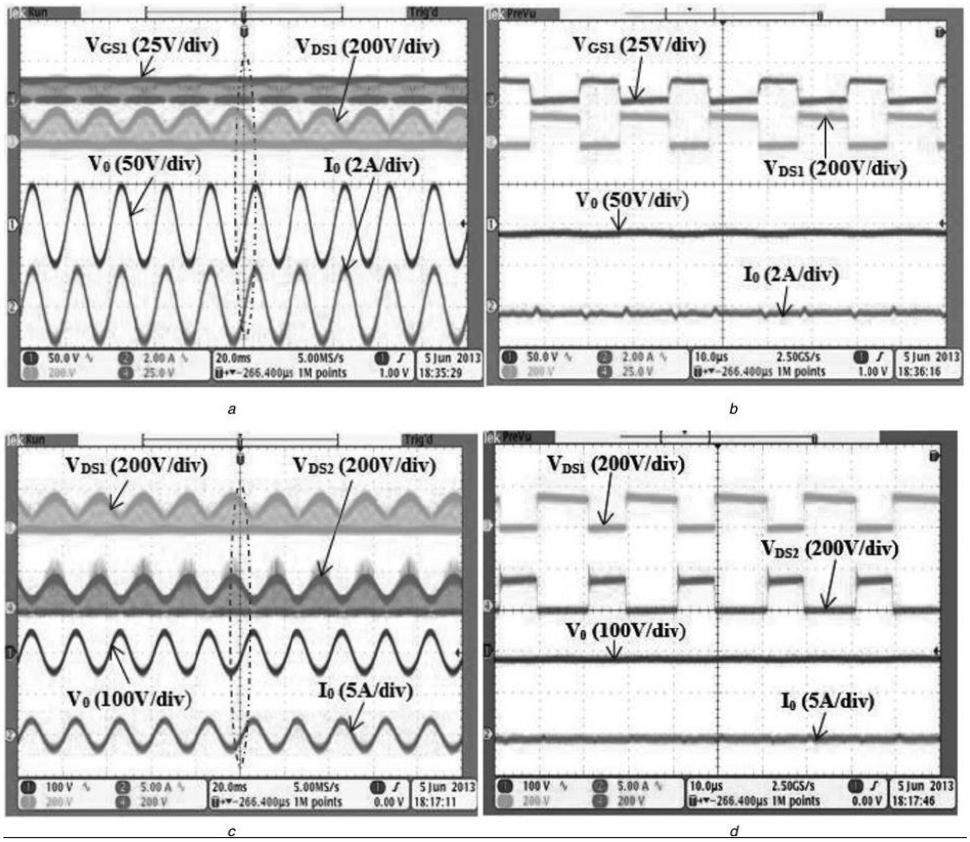

Fig. 5 *Experimental waveforms for R load*

a Gate to source voltage, drain to source voltage, output voltage and output current
b Zoomed in waveform of gate to source voltage, drain to source voltage, output voltage and output current
c Drain to source voltage of two switches, output voltage and output current
d Zoomed in waveform of drain to source voltage of two switches, output voltage and output current

Figs. 7*a* and *b* display that for both the *R* and *R–L* loads condition, the input voltage V_{in} is almost constant and contains no high frequency variation. As a consequence, the generation of common mode voltage is minimised, which in turns results in reduction of common-mode leakage current. The voltage across capacitor C_1, current through inductor L_1, output voltage and output current of the inverter for both the *R* and *R–L* loads are shown in Figs. 7*c* and *d*, respectively. Both the figures notified, voltage developed across the capacitor C_1 followed by the inductor current I_{L_1} and inductor current is approximately twice the output current for both the load conditions.

Fig. 8 illustrates the condition when a single-phase induction motor has been applied as load at the output of inverter. Fig. 8*a* shows the waveforms of input voltage V_{in}, output voltage V_o and output current I_o at the starting condition of the motor. Meanwhile, Fig. 8*b* shows the same waveforms when the motor operates at one of the steady-state condition of motor. It is seen from these two figures that, motor draws high current during starting as single-phase induction motor requires high current density at the auxiliary winding during starting. For this reason, the output voltage and current of the inverter have some distortion at the starting condition. Whereas, at steady-state condition it draws less current from inverter which in turns, reduce the distortion of output voltage and current. It can also be seen that, the output current is lagging the output voltage for both the starting and running conditions for the motor load.

THD and harmonic spectrum of the output voltage and current for *R*, *R–L* and motor loads (starting and steady-state condition) are displayed in Figs. 9*a–d*, respectively. It can be depicted from Figs. 9*a* and *b* that, for *R* load the inverter produces RMS output voltage of 35.94 V with THD of 4.506% and RMS output current of 1.30 A with THD of 4.50%. While for *R–L* load the inverter produces RMS output voltage of 35.76 V with THD of 1.16% and RMS output current of 0.315 A with THD of 1.68%. In case of *R* load, the inverter supplies real power of 46.76 W at unity power factor. On the other hand, the inverter supplies real power of 3.68 W and reactive power of 10.62var for *R–L* load. In addition, for both the *R* and *R–L* loads condition, THD's are within the limit (<5%), no occurrence of DC current component and percentage of

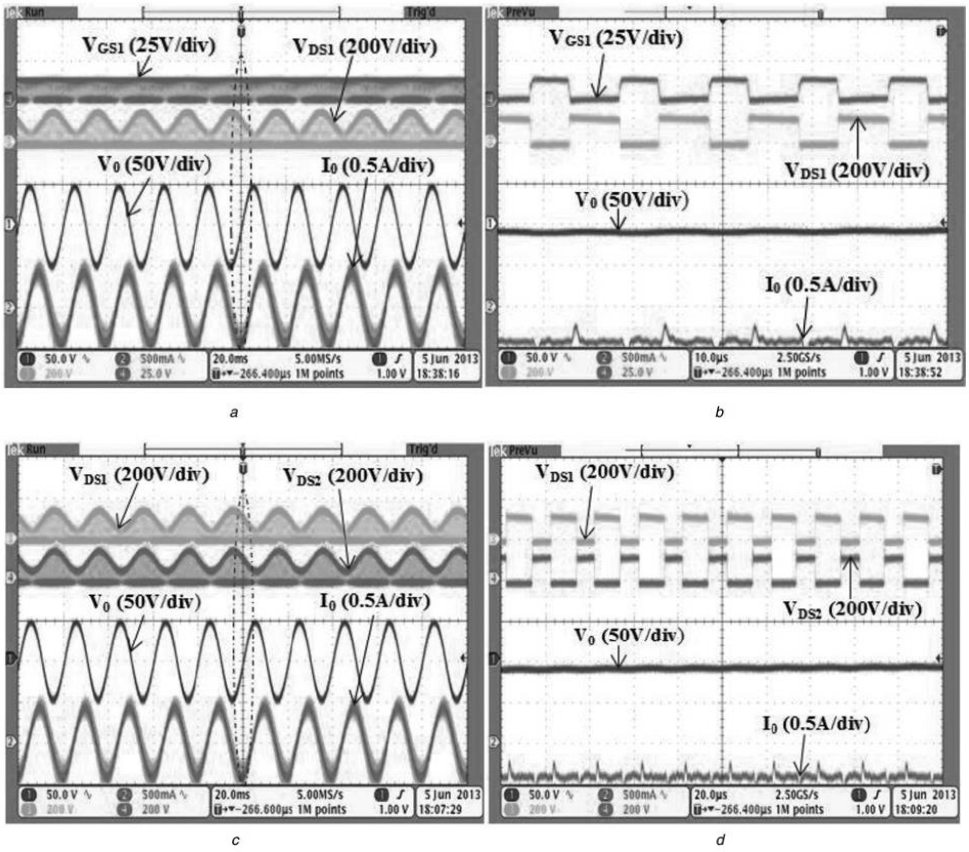

Fig. 6 *Experimental waveforms for R–L load*

a Gate to source voltage, drain to source voltage, output voltage and output current
b Zoomed in waveform of gate to source voltage, drain to source voltage, output voltage and output current
c Drain to source voltage of two switches, output voltage and output current
d Zoomed in waveform of drain to source voltage of two switches, output voltage and output current

higher order harmonic components are very negligible at the output. On the contrary, Fig. 9*c* shows the THD and harmonic spectrum at the starting condition of motor load. Whereas, Fig. 9*d* shows the THD and harmonic spectrum when the motor load has been operated at one of the steady-state conditions of motor. At the starting of the motor, the inverter produces RMS output voltage of 32.26 V with THD of 9.93% and RMS output current of 2.65 A with THD of 10.49%. Whereas, at the steady-state condition the inverter produces RMS output voltage of 40.25 V with THD of 0.834% and RMS output current of 0.38 A with THD of 5.48%. At the starting of motor, the output voltage and current of inverter contains high THD because, motor stator winding of single-phase induction have high harmonic distortion during starting [40]. However, during the steady-state condition, the output voltage contains very less THD and current contains slightly greater than 5% as the motor does not run in rated speed here. It is also seen from these figures that, the inverter supplies real power of 68.70 W and reactive power of 50.91var at 0.80 power factor during starting of motor load. Furthermore, during the steady-state condition of motor, the inverter supplies real power of 4.90 W and reactive power of 14.27var at 0.33 power factor. In addition, the inverter is capable of supplying not only real power but also reactive power at low power factor and output contains no DC components as well as higher order harmonics.

Finally, the prototype of the inverter has interfaced with the low voltage utility grid to observe the power transfer in synchronous mode. During interfacing with the grid in laboratory condition the utility grid voltage has been taken 50 V_{ac} with frequency of 50 Hz. Synchronous operation between grid voltage and inverter output voltage is shown in Fig. 10*a*. Fig. 10*b* shows the experimental waveforms of grid voltage and grid current during full-load condition. It shows that, there is no phase difference between the sinusoidal output current of inverter or grid current and the grid voltage. Experimental waveforms of input voltage V_{in}, voltage across capacitor C_1 and output current I_o of the inverter during grid interfacing are shown in Fig. 10*c*. This figure depicts that, during grid tied application input voltage is almost constant and contains no high frequency variation, which means that the generation of common mode voltage is minimised, which results in the generation of common